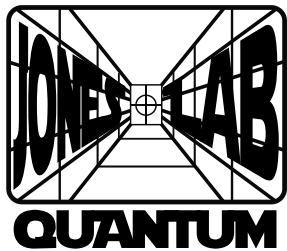


Using Quantum Hardware Speed Limits to Improve Basis Gate Selection

Evan McKinney[†],
C. Zhou[§], M. Xia[§], M. Hatridge[§], A.K. Jones[†]



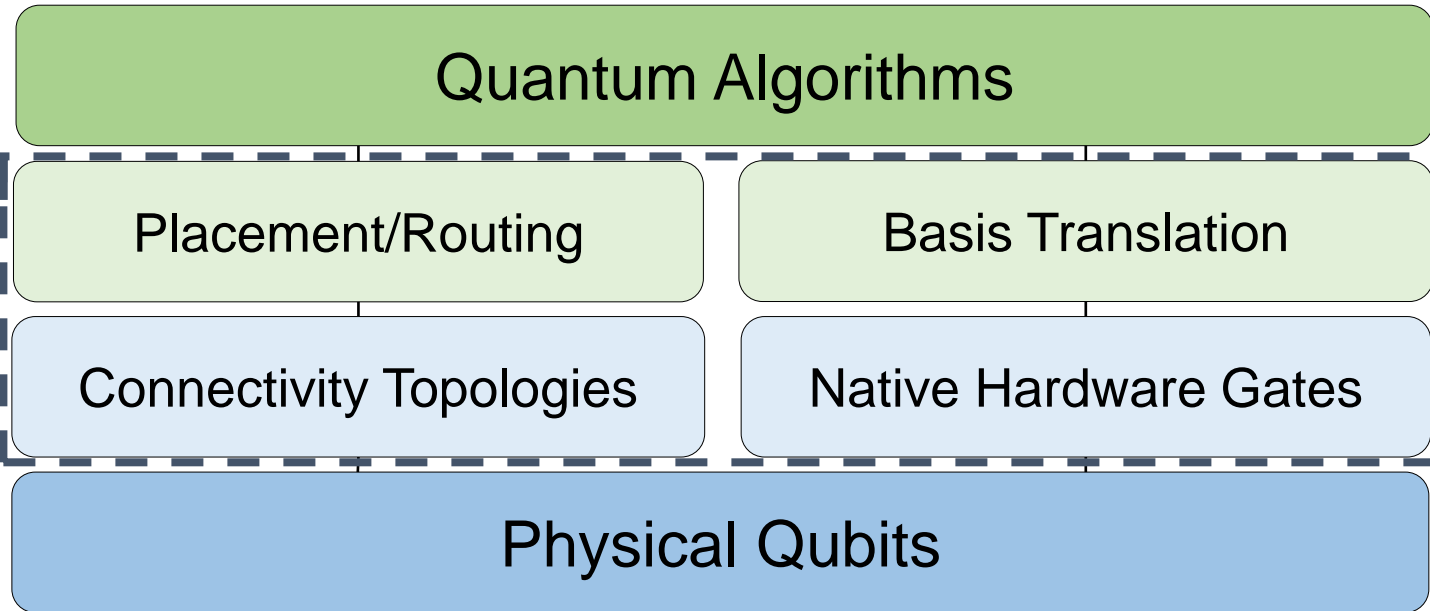
[†]Department of Electrical and Computer Engineering, University of Pittsburgh
[§]Department of Physics and Astronomy, University of Pittsburgh



ISCA 2023



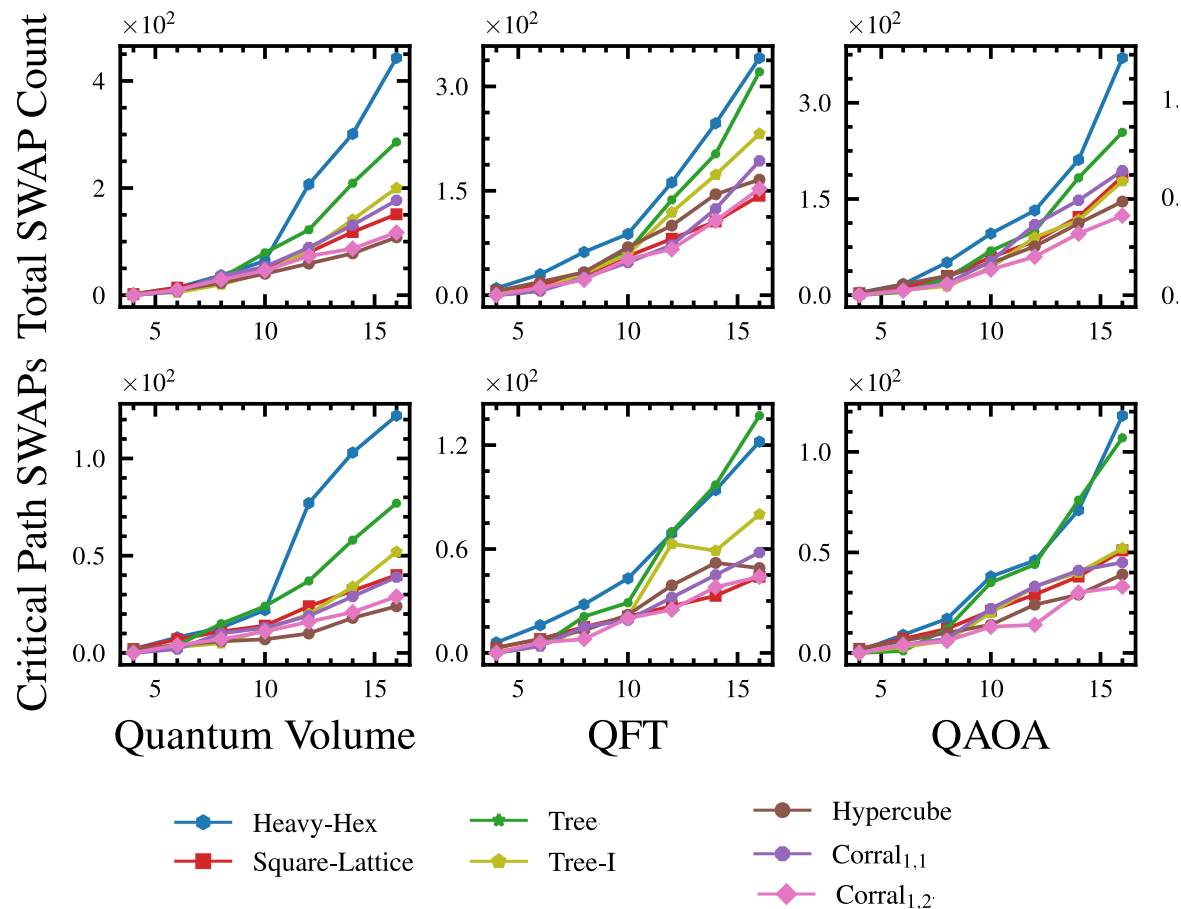
Transpilation ←



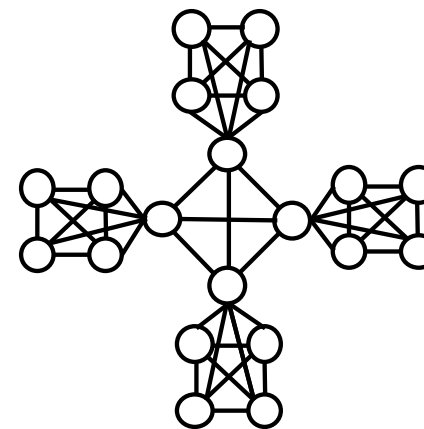
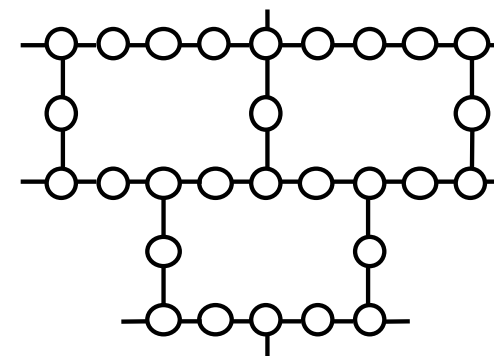
- Physics constrains possible topologies and basis gates
- Prioritize improving qubit and gate fidelities

What we've done

- Transpile circuits to Hatlab connectivity
- Co-design study topology networks

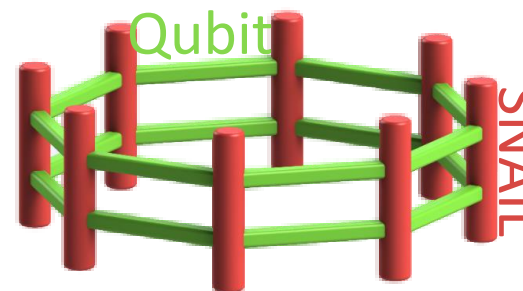
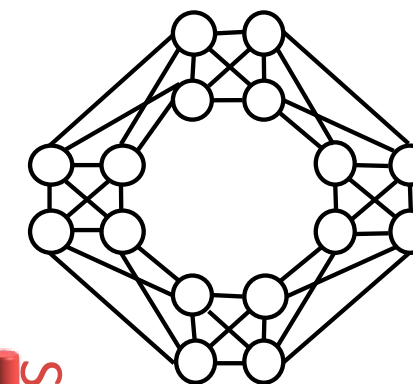


(a) Heavy-Hex, 28-qubits



(b) Tree, 20-qubits

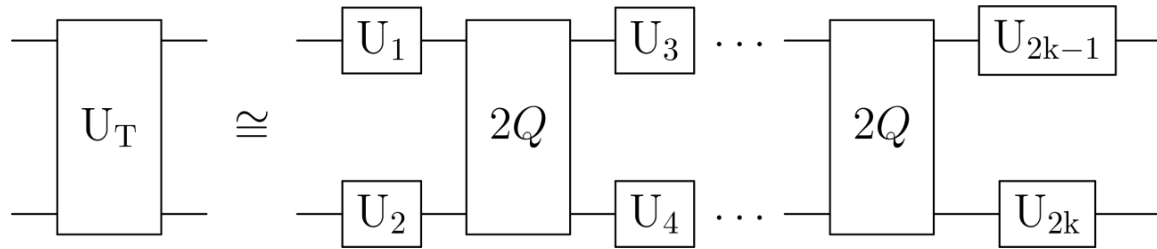
(c) Corral, 16-qubits



(d) Corral realization via SNALS

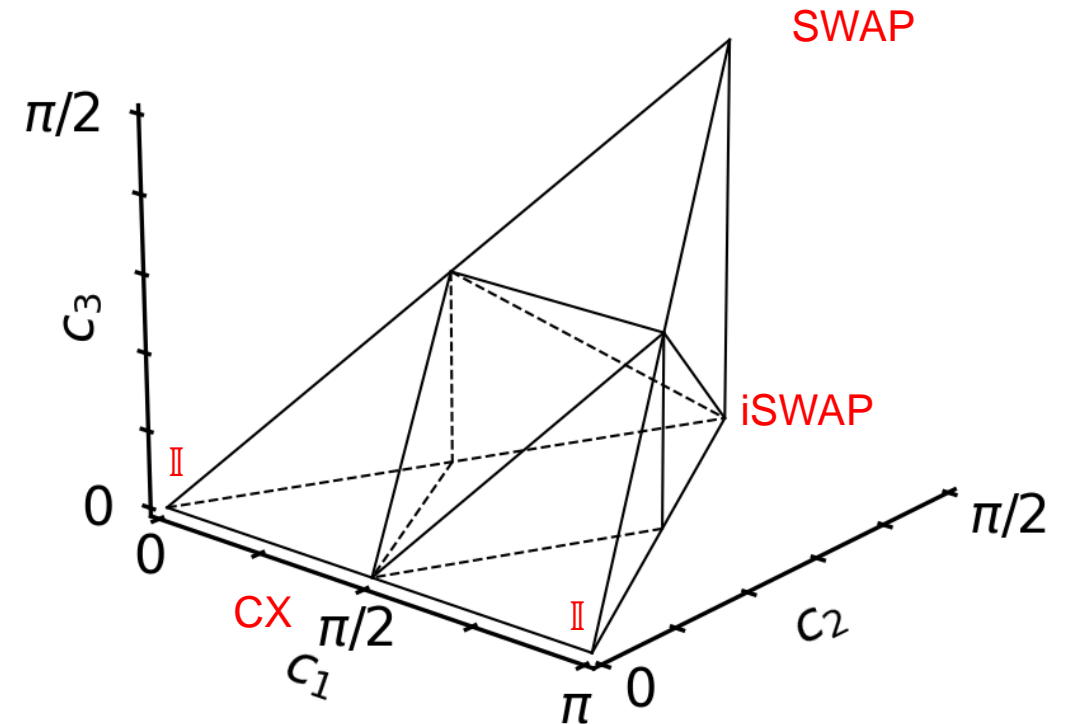
Two-qubit basis gates

- Decompose all algorithm gates into new basis using repeated applications



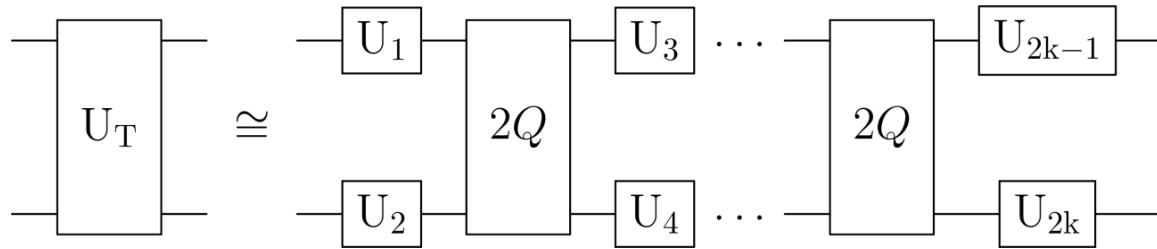
- An optimal basis gate *reduces overall duration*
 - Powerful gates need less applications
 - Fidelity limited by decoherence in time

- Weyl Chamber visualizes the set of all 2Q gates



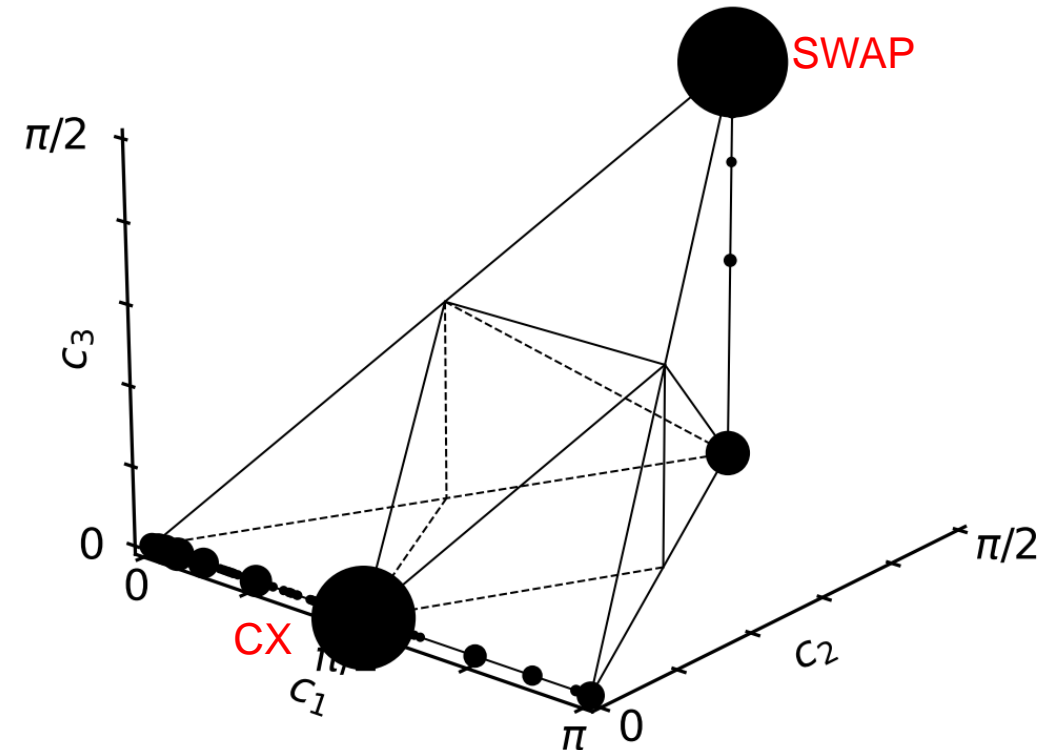
Two-qubit basis gates

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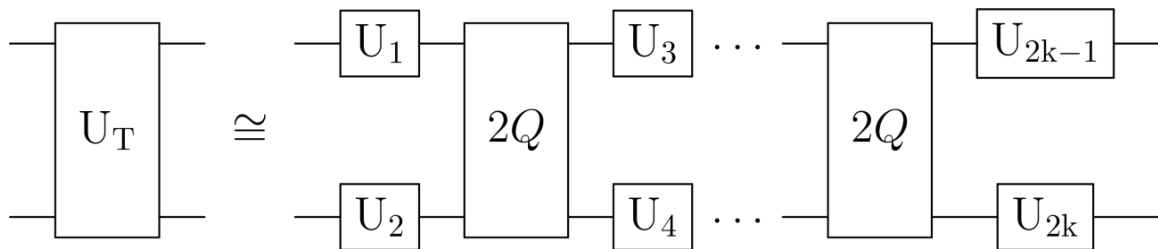
- Weyl Chamber visualizes the set of all 2Q gates



- NISQ algorithms dominated by CX and $SWAP$ gates

Two-qubit basis gates

- Decompose all algorithm gates into new basis using repeated applications

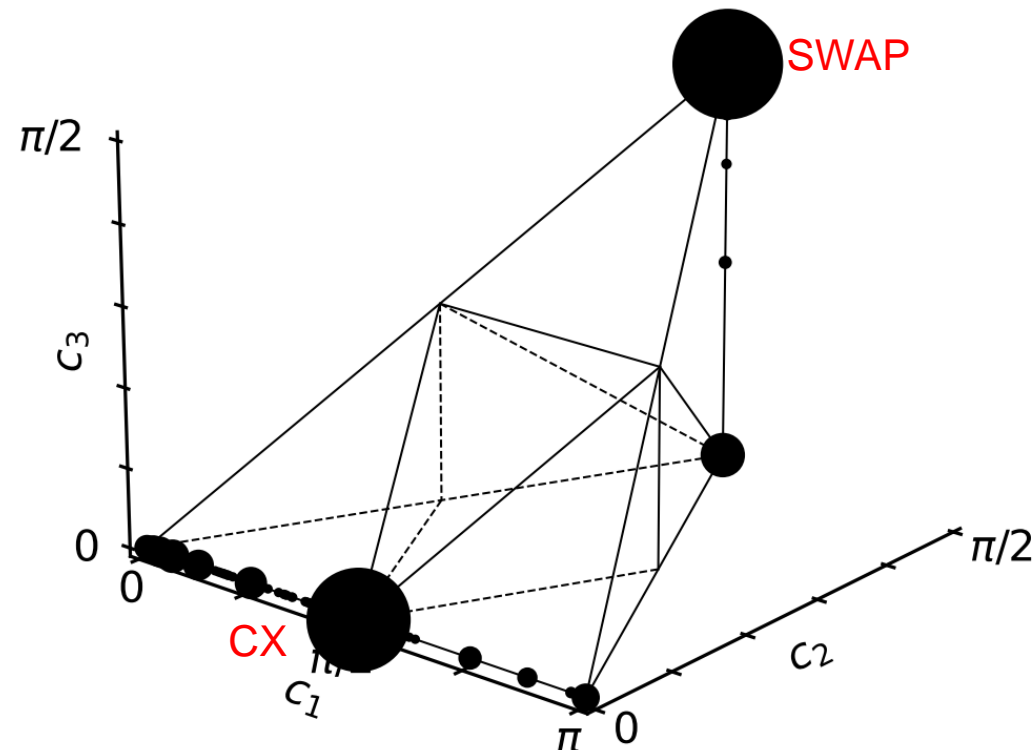


- An optimal basis gate *reduces overall duration*

- Powerful gates need less applications
- Fidelity limited by decoherence in time

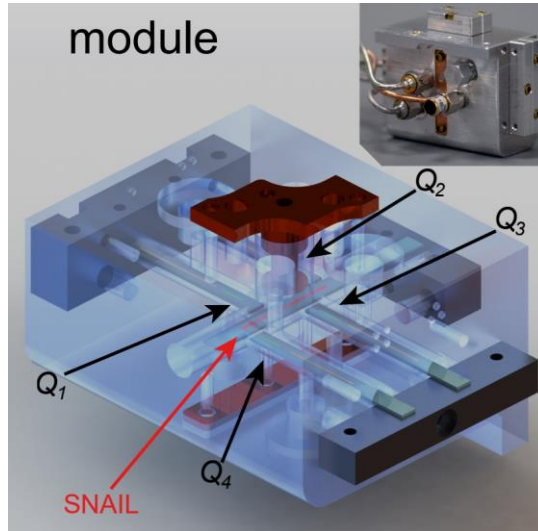
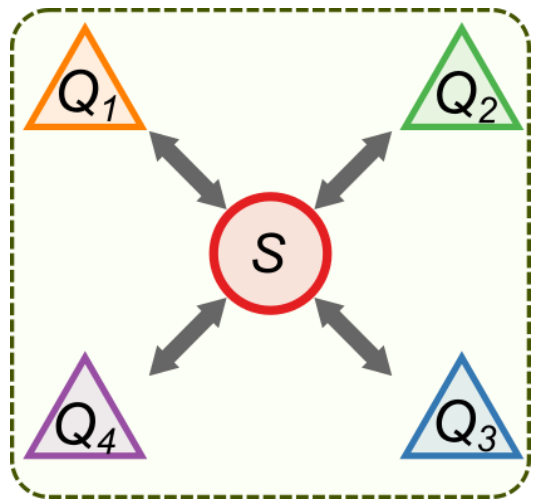
- **Goal: Use both decomposition efficiency and hardware latency = overall duration**

- Weyl Chamber visualizes the set of all 2Q gates



- NISQ algorithms dominated by CX and SWAP gates

Four qubit SNAIL-based quantum module



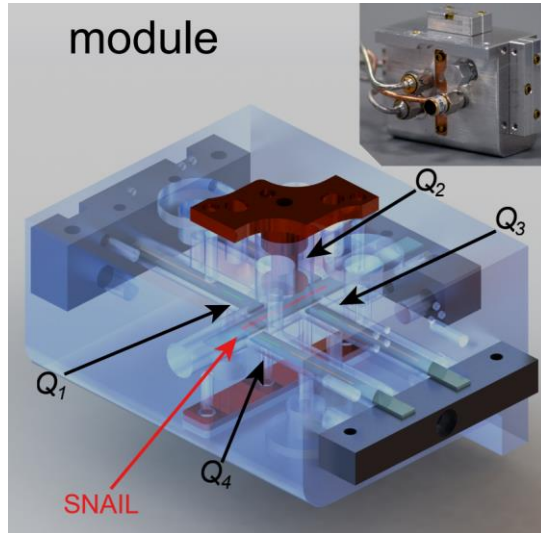
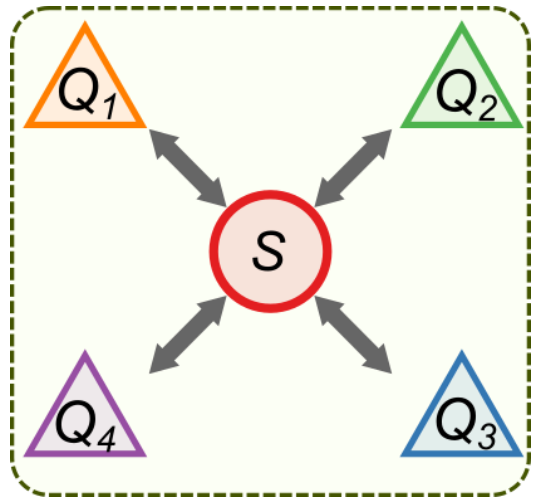
➤ Engineerable interactions yields a basis gate design-space

$$\hat{H} = g_c(e^{i\phi_c} a^\dagger b + e^{-i\phi_c} ab^\dagger) + g_g(e^{i\phi_g} ab + e^{-i\phi_g} a^\dagger b^\dagger)$$

Xia, et al. **APS March Meeting** (2023)

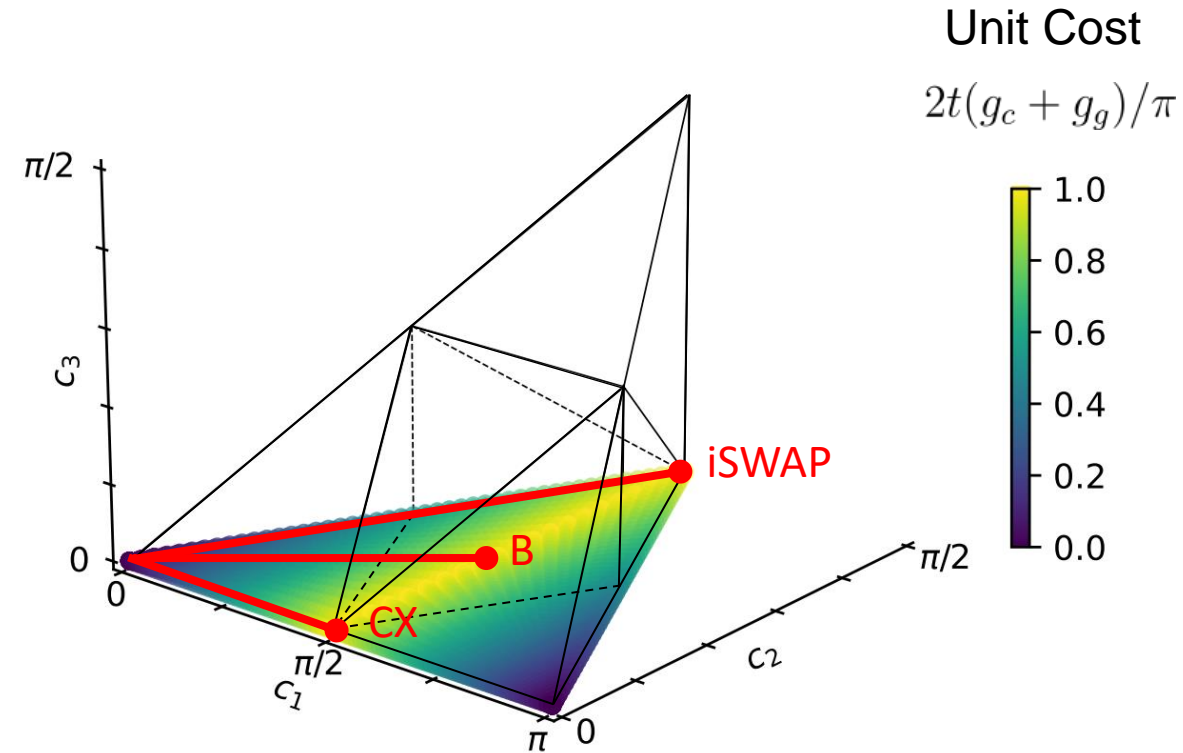
Zhou, et al. **npj Quantum Inf** 9, 54 (2023).

Four qubit SNAIL-based quantum module

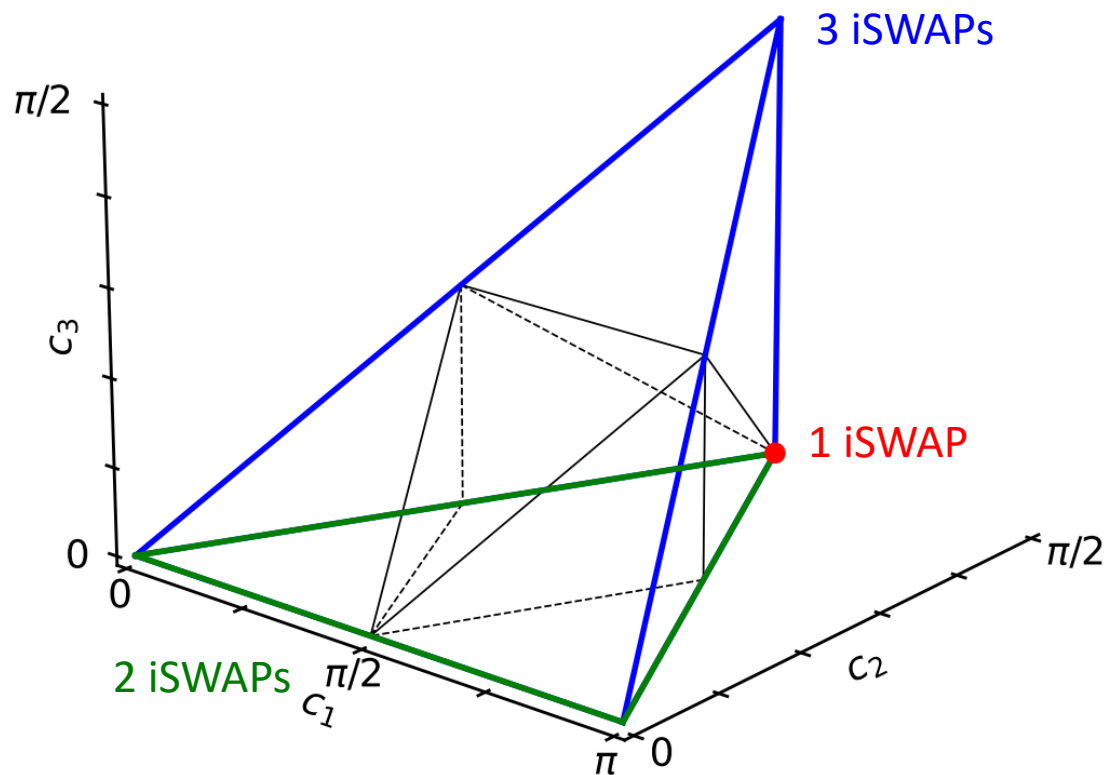


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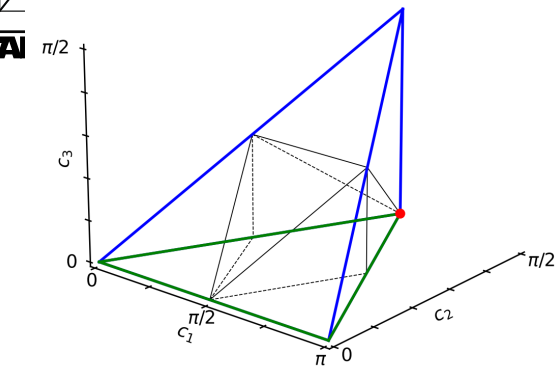
Basis coverage volumes



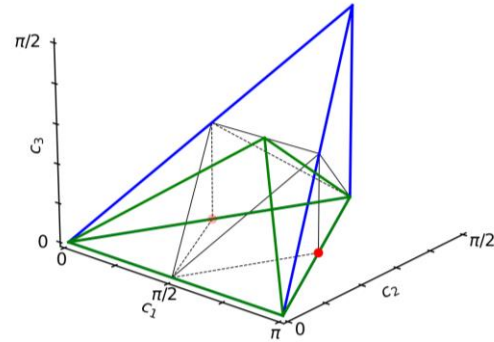
- **Monodromy polytopes** finds minimum gate applications for any 2Q target gate
- A single gate is locally equivalent to itself
- SWAP is the most expensive target

Target\Basis	iSWAP
CNOT	2.0
SWAP	3.0
Haar	3.0

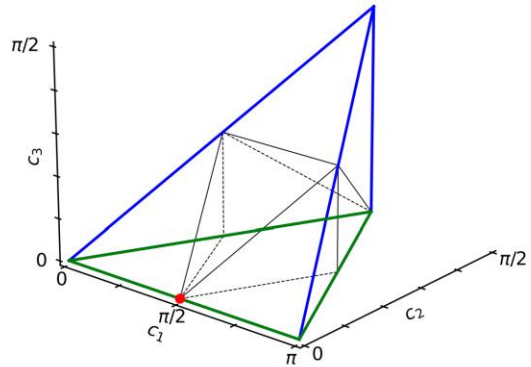
Basis coverage volumes



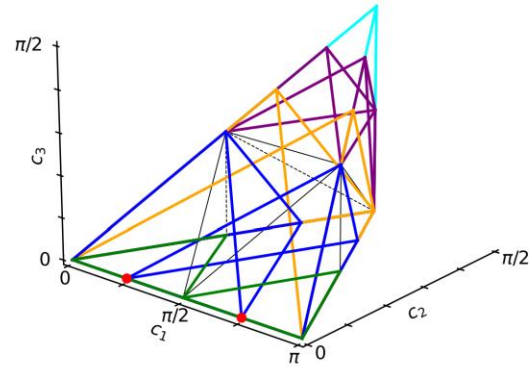
(a) i SWAP



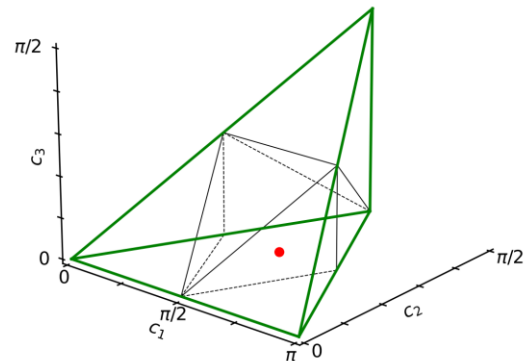
(b) \sqrt{i} SWAP



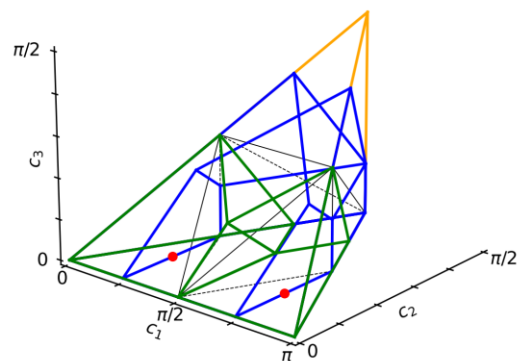
(c) CNOT



(d) \sqrt{C} NOT



(e) B



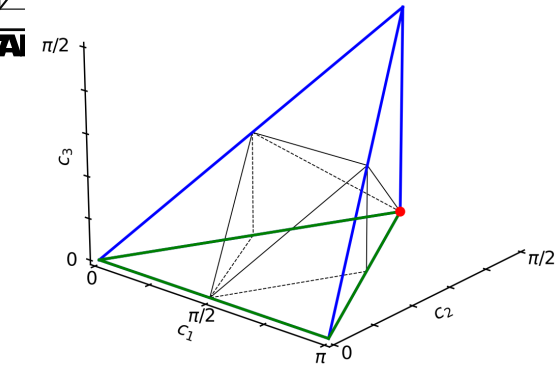
(f) \sqrt{B}

- **Monodromy polytopes** finds minimum gate applications for any 2Q target gate
- A single gate is locally equivalent to itself
- SWAP is the most expensive target

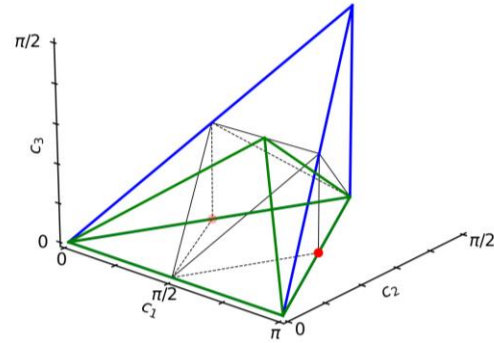
Decomposition *gate count* costs

Target\Basis	i SWAP	\sqrt{i} SWAP	CX	\sqrt{CX}	B	\sqrt{B}
CNOT	2.0	2.0	1.0	2.0	2.0	2.0
SWAP	3.0	3.0	3.0	6.0	2.0	4.0
Haar	3.0	2.2	3.0	3.5	2.0	3.1

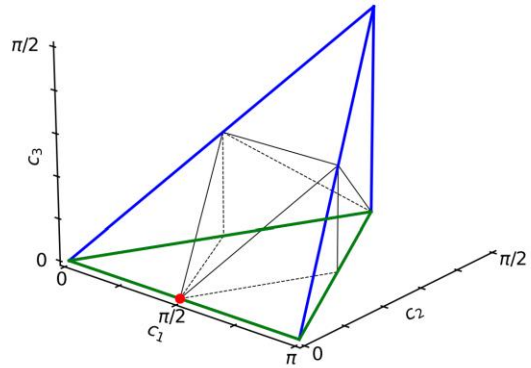
Basis coverage volumes



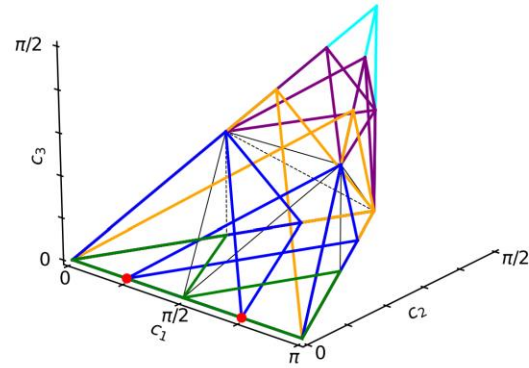
(a) i SWAP



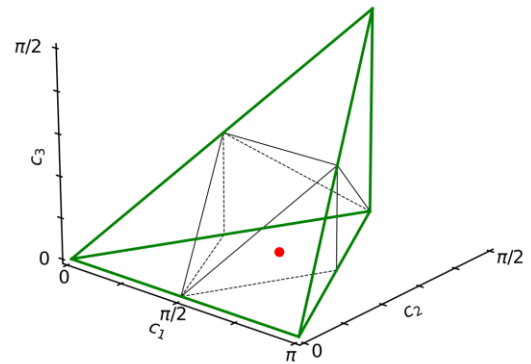
(b) \sqrt{i} SWAP



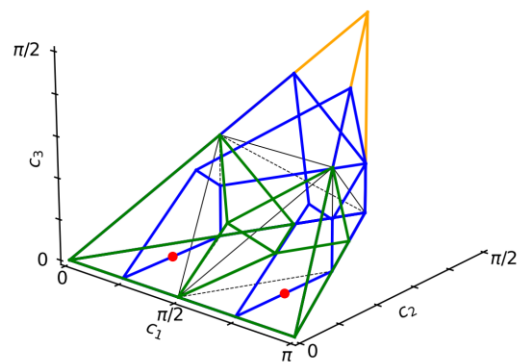
(c) CNOT



(d) \sqrt{C} NOT



(e) B



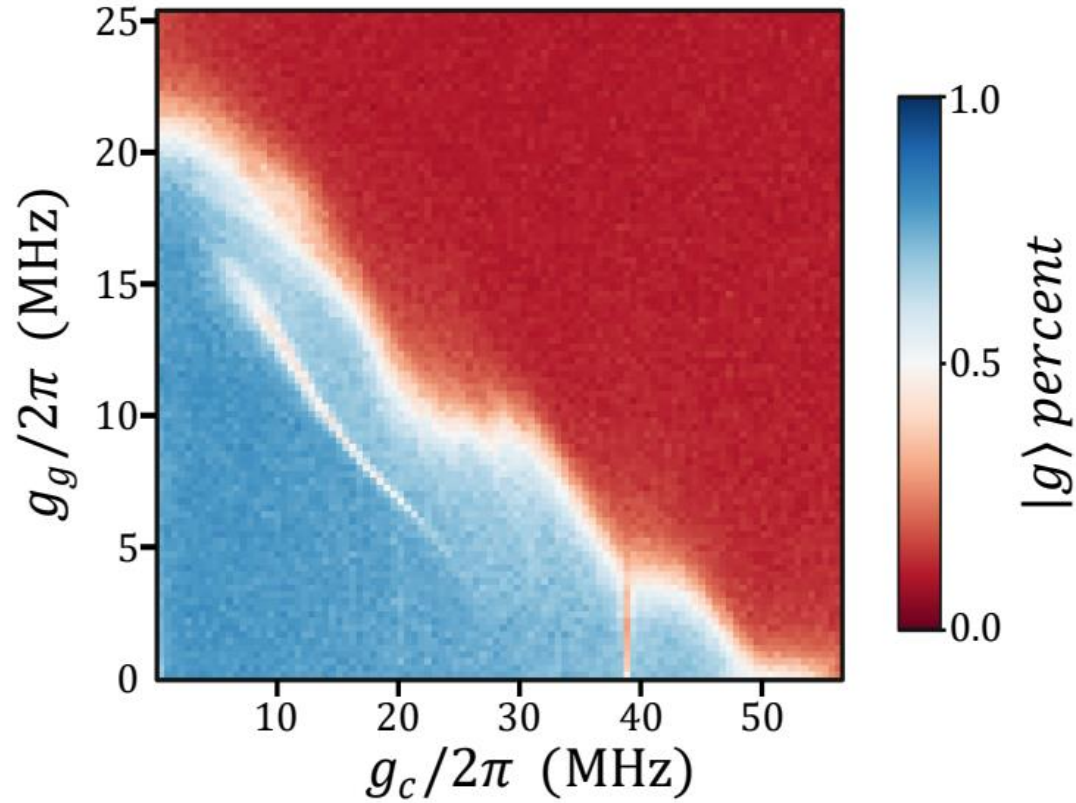
(f) \sqrt{B}

- **Monodromy polytopes** finds minimum gate applications for any 2Q target gate
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Decomposition *gate count* costs

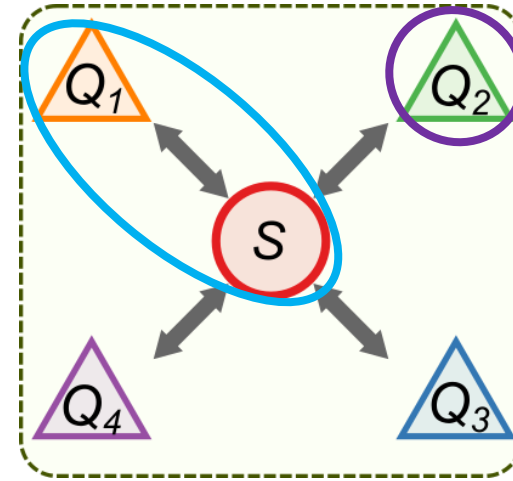
Target\Basis	i SWAP	\sqrt{i} SWAP	CX	\sqrt{CX}	B	\sqrt{B}
CNOT	2.0	2.0	1.0	2.0	2.0	2.0
SWAP	3.0	3.0	3.0	6.0	2.0	4.0
Haar	3.0	2.2	3.0	3.5	2.0	3.1

Hardware speed limits



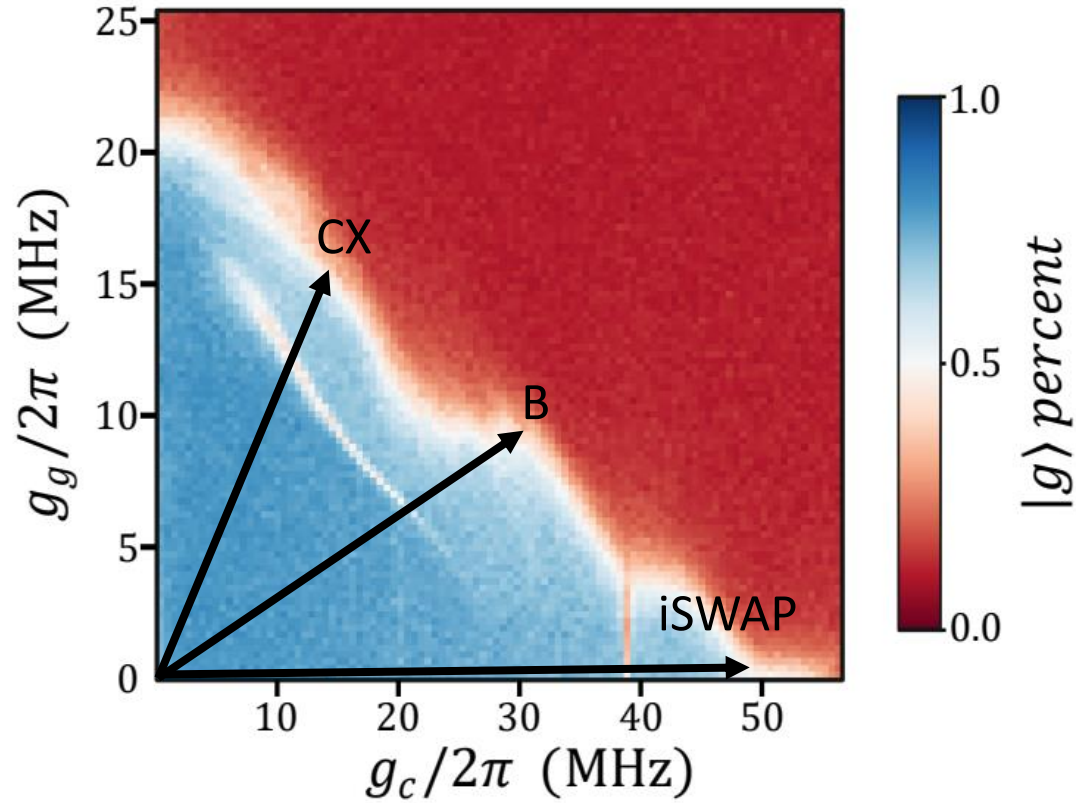
Limitation of SNAIL when driving both gain and conversion

Module



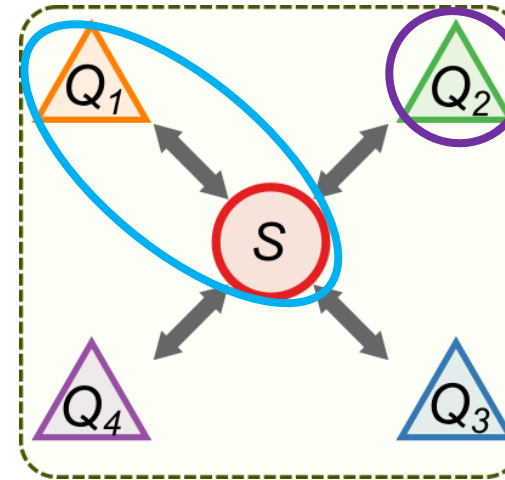
Drives applied between SNAIL and qubit

Measure second qubit to witness SNAIL breakpoint



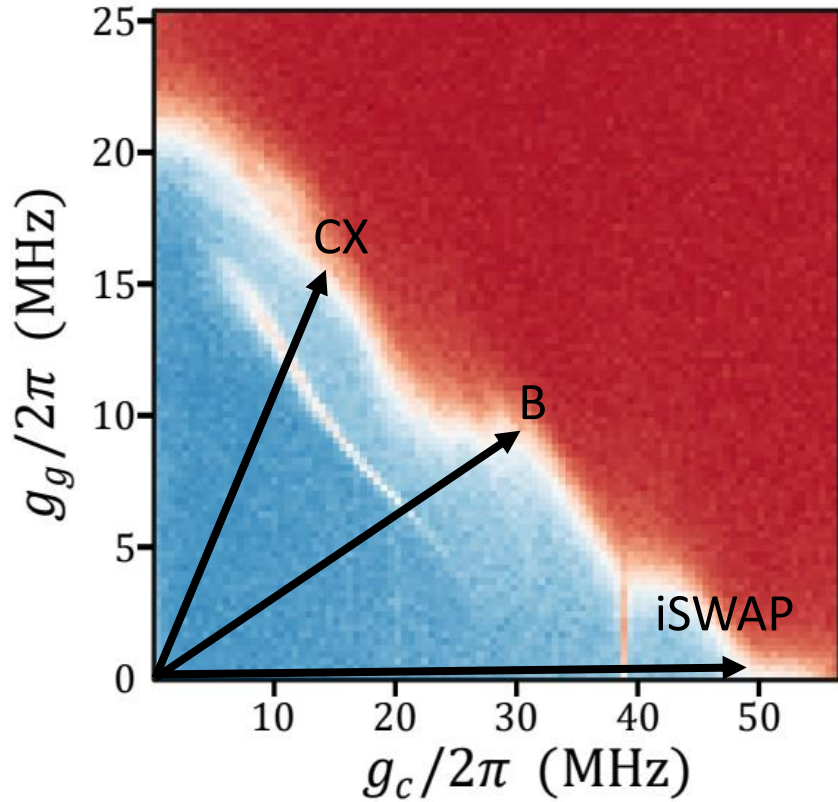
Limitation of SNAIL when driving both gain and conversion

Module



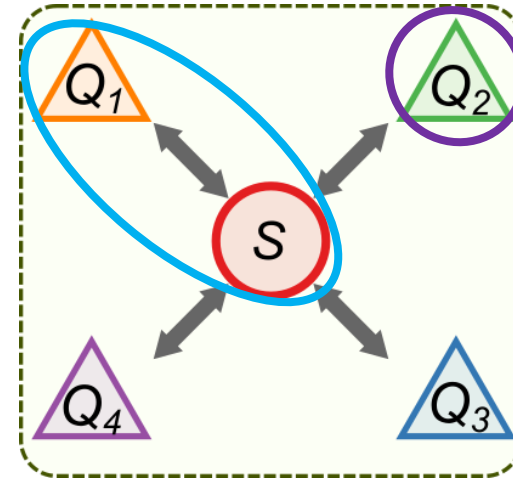
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Limitation of SNAIL when driving both gain and conversion

Module

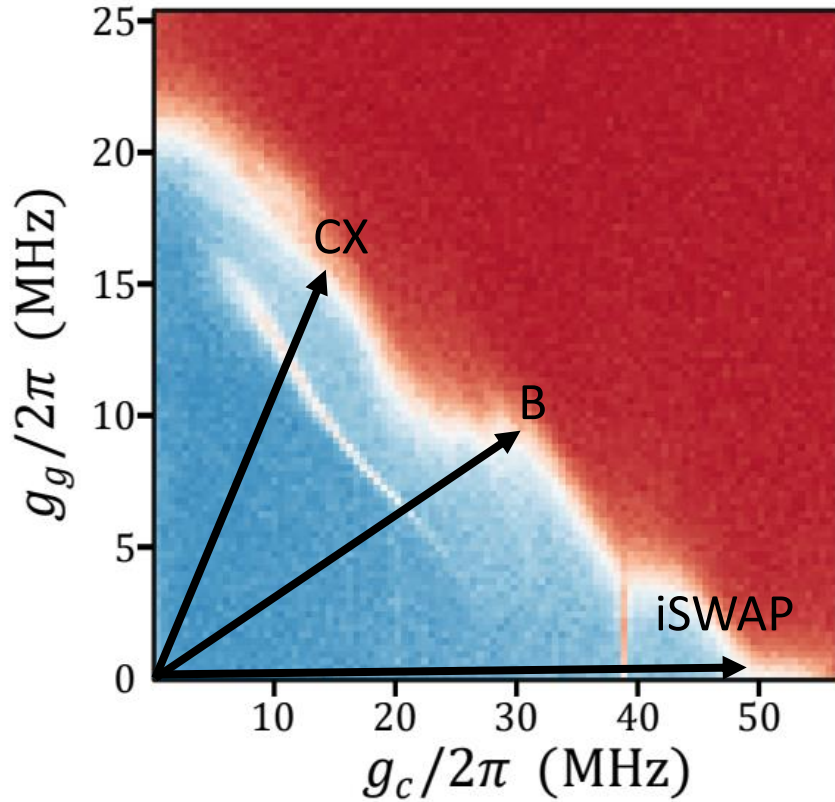


Drives applied between SNAIL and qubit

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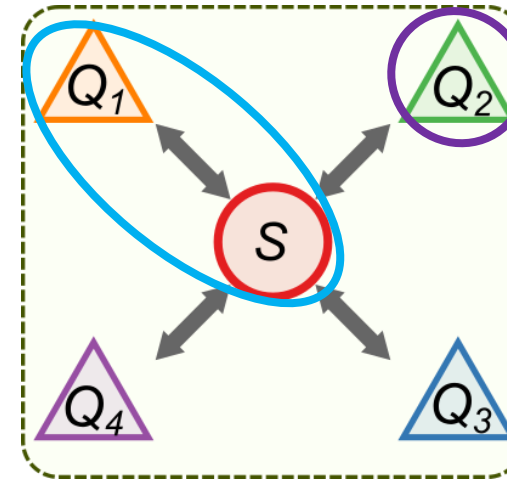
Decomposition normalized *duration* costs

Target\Basis	iSWAP	\sqrt{iSWAP}	CX	\sqrt{CX}	B	\sqrt{B}
Duration	1.0	0.5	1.8	0.9	1.4	0.7
CNOT	2.0	1.0	1.8	1.8	2.8	1.4
SWAP	3.0	1.5	5.4	5.4	2.8	2.8
Haar	3.0	1.1	5.4	3.2	2.8	2.2



Limitation of SNAIL when driving both gain and conversion

Module

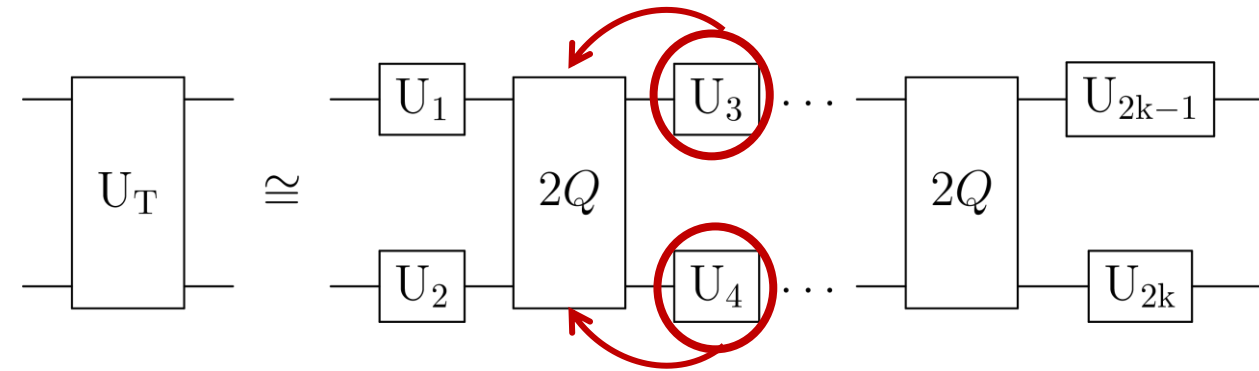


Drives applied between SNAIL and qubit

Measure second qubit to witness SNAIL breakpoint

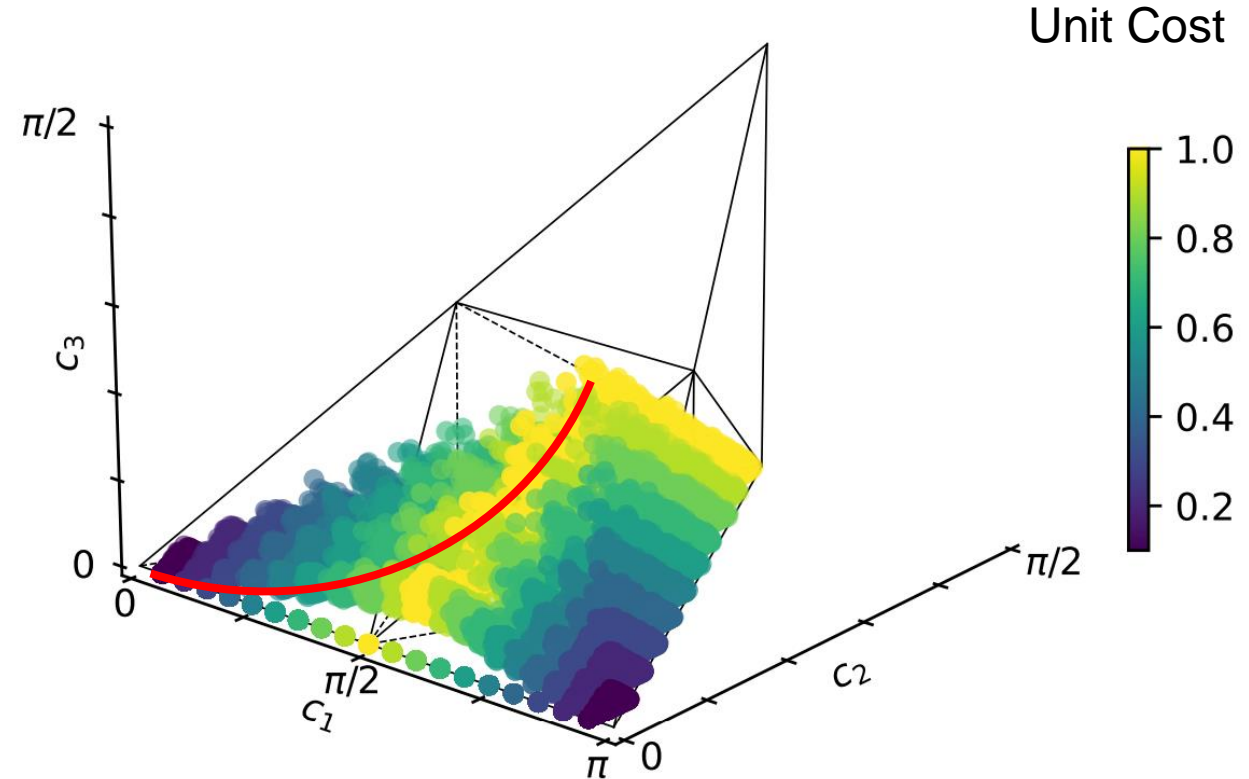
Decomposition normalized *duration* costs

Target\Basis	iSWAP	\sqrt{iSWAP}	CX	\sqrt{CX}	B	\sqrt{B}
Duration	1.0	0.5	1.8	0.9	1.4	0.7
CNOT	2.0	1.0	1.8	1.8	2.8	1.4
SWAP	3.0	1.5	5.4	5.4	2.8	2.8
Haar	3.0	1.1	5.4	3.2	2.8	2.2



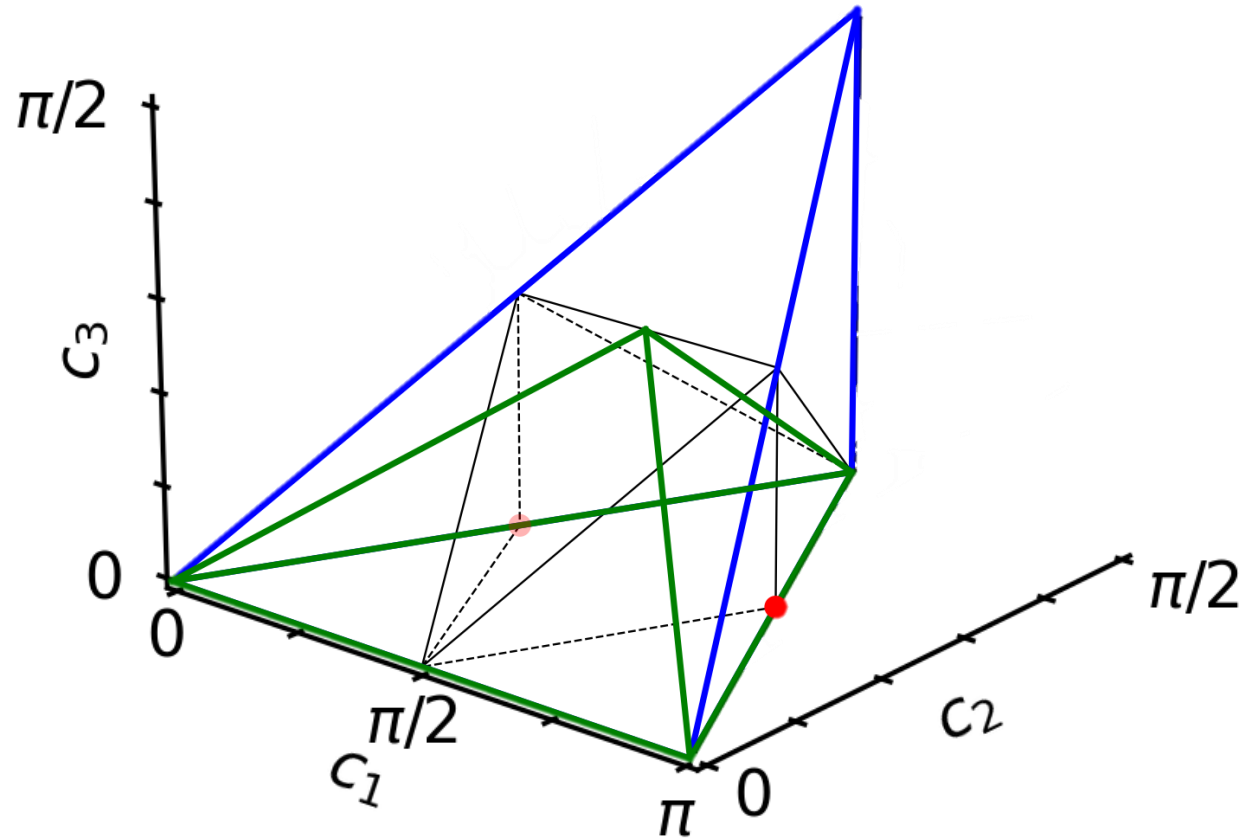
- Drive qubits independently from the SNAIL in discrete time steps equivalent to basis gate duration

$$\hat{H} = g_c(e^{i\phi_c} a^\dagger b + e^{-i\phi_c} a b^\dagger) + g_g(e^{i\phi_g} a b + e^{-i\phi_g} a^\dagger b^\dagger) + \epsilon_1(t)(a + a^\dagger) + \epsilon_2(t)(b + b^\dagger)$$

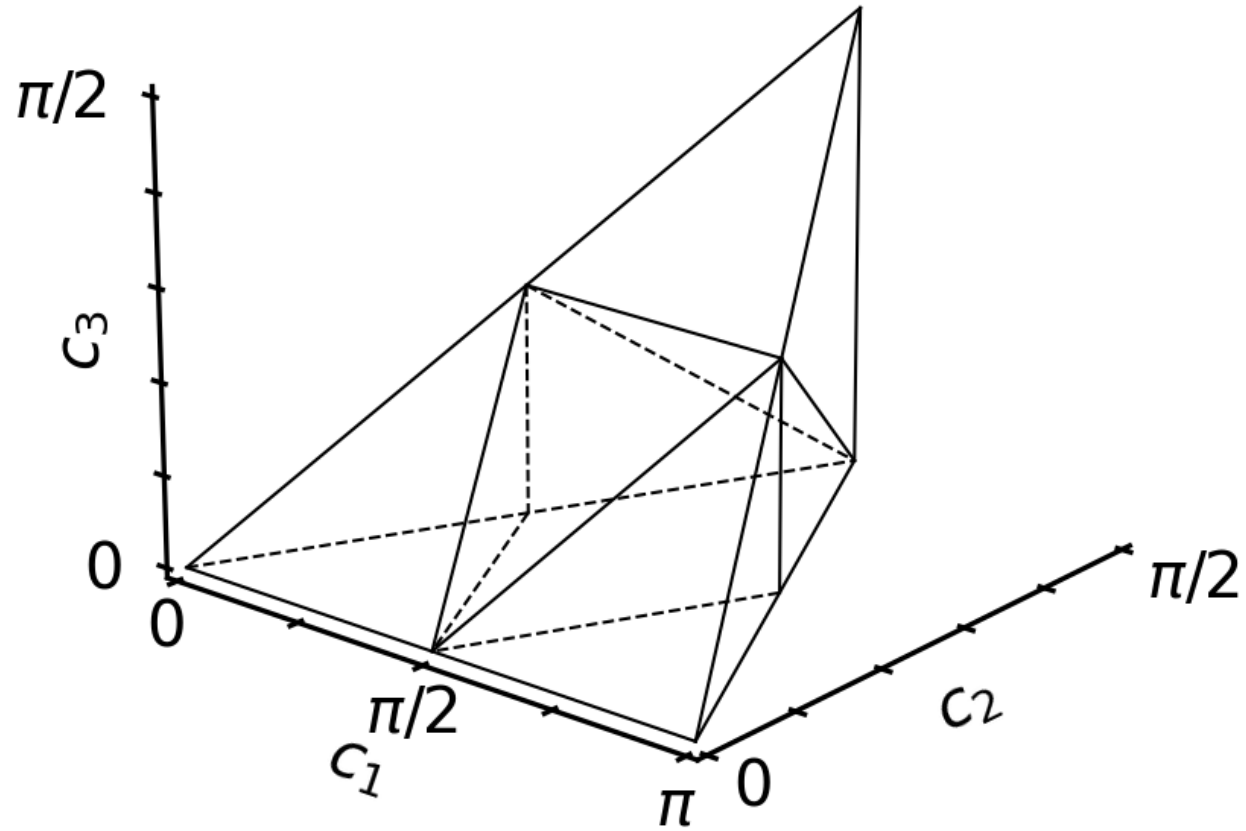


- Parallel-Drive “steers” to previously inaccessible regions

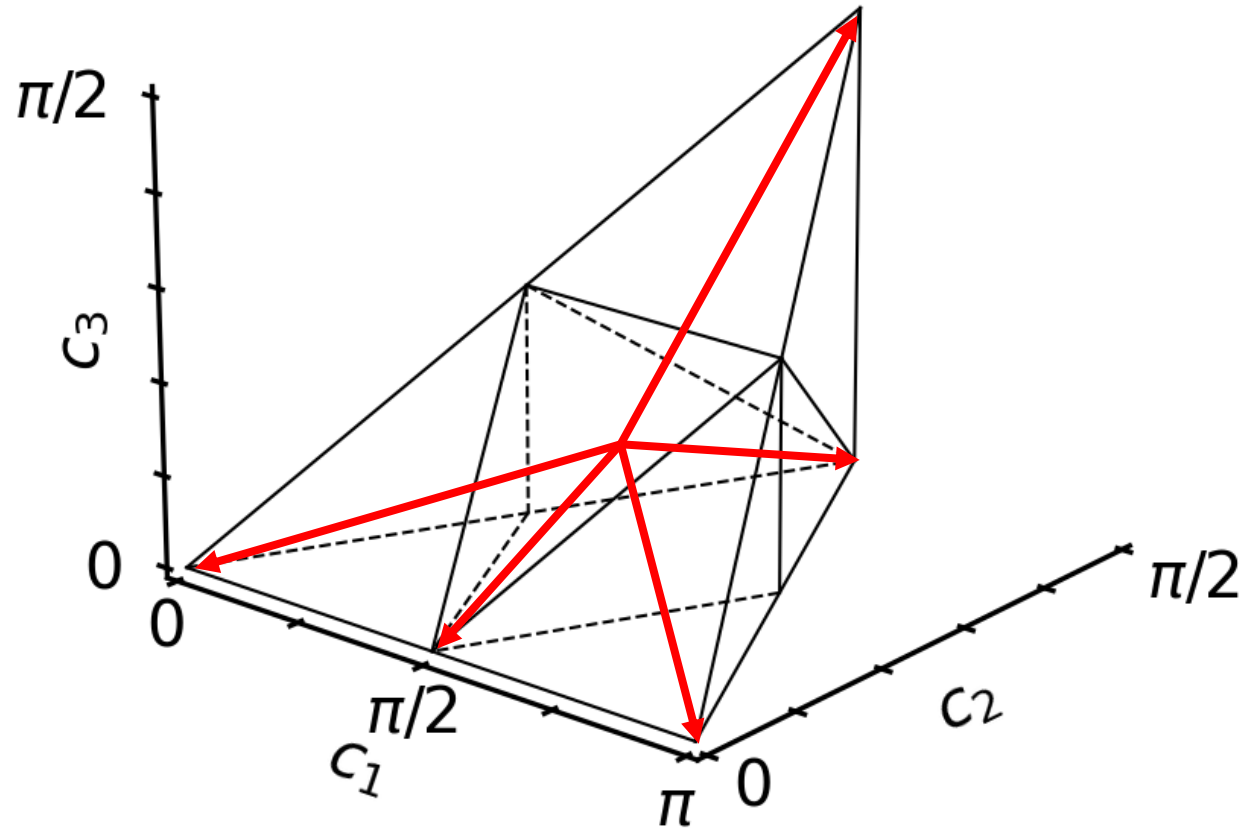
Extended basis coverage volumes



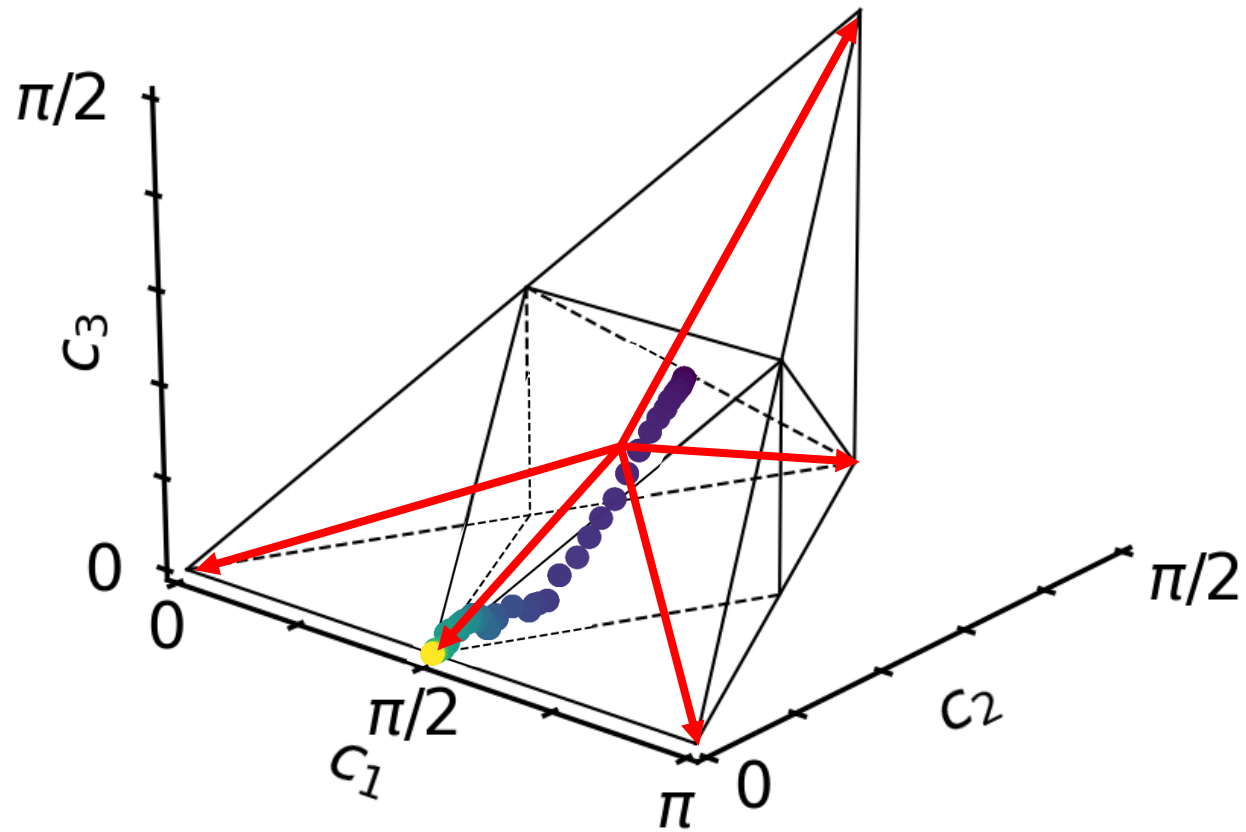
Extended basis coverage volumes



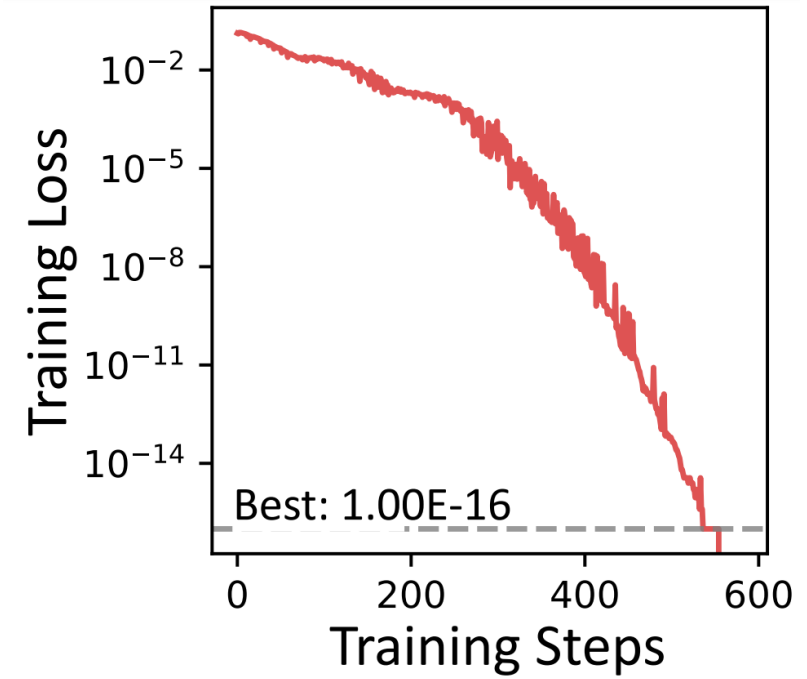
Extended basis coverage volumes



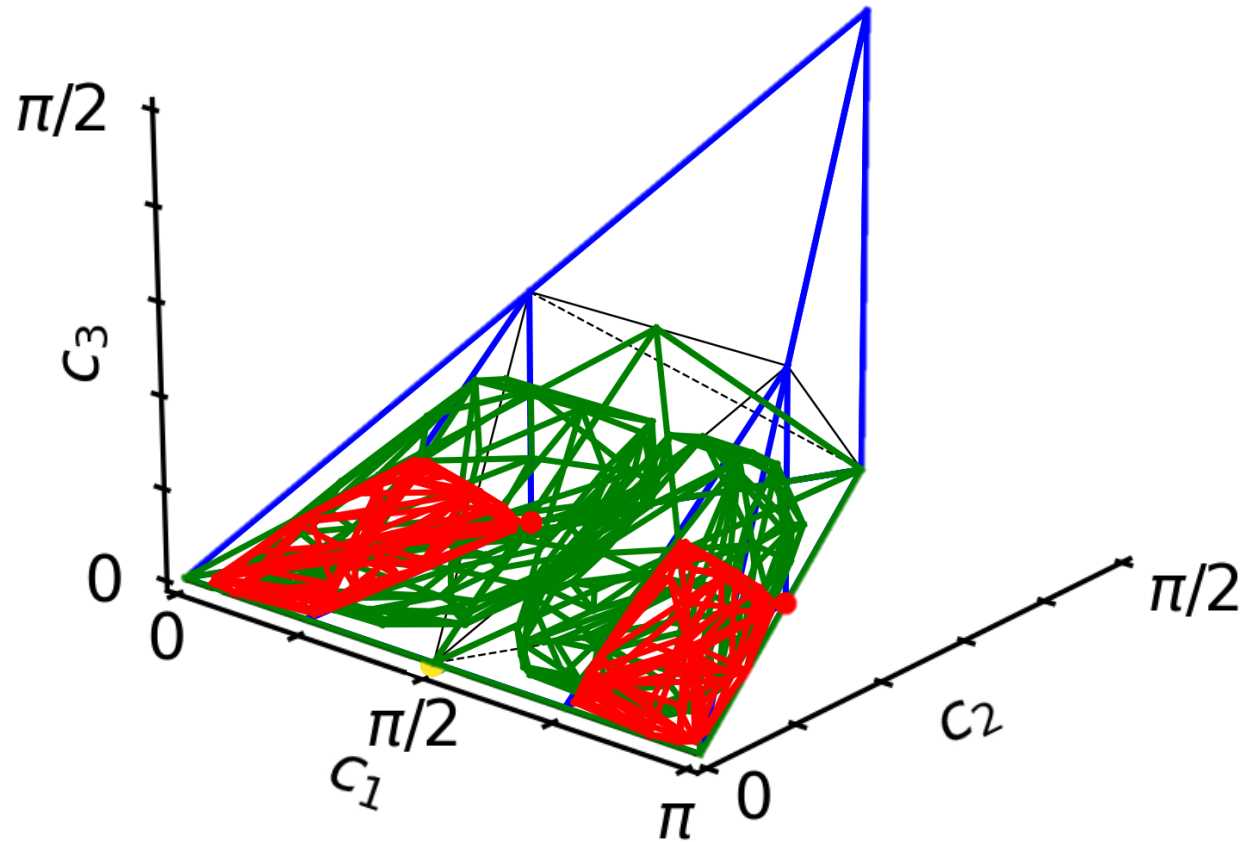
Extended basis coverage volumes



- Nelder-Mead optimization over Makhlin invariants functional

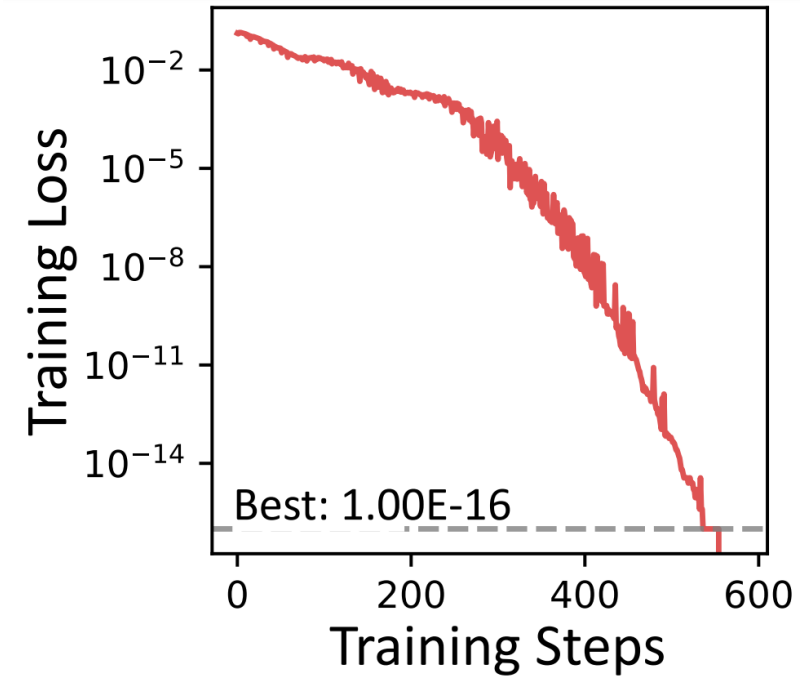


Extended basis coverage volumes

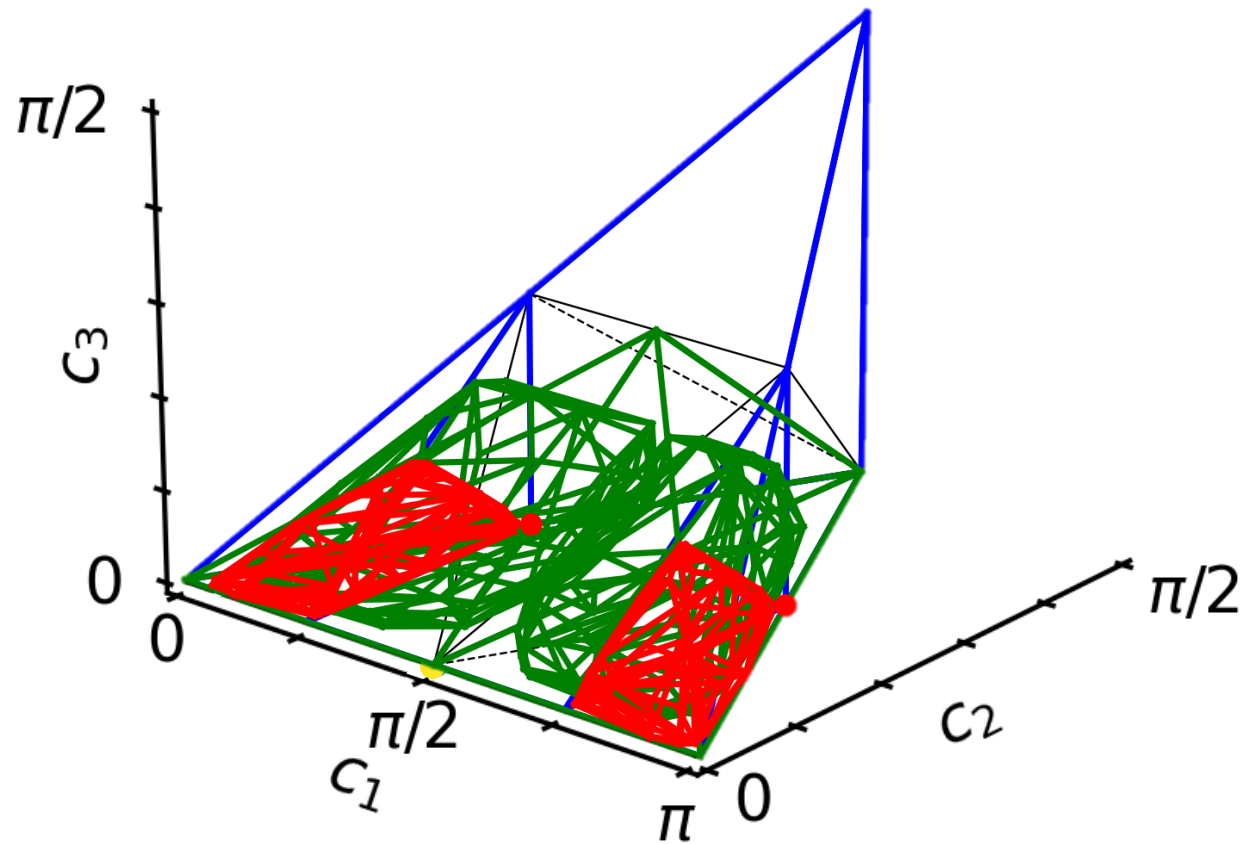


➤ Single gates have non-zero volume!

➤ Nelder-Mead optimization over Makhlin invariants functional

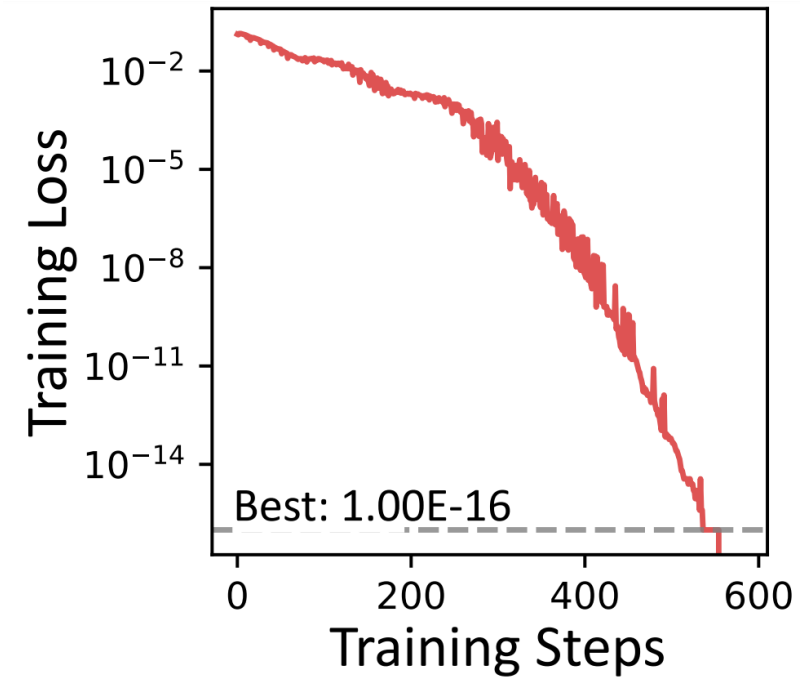


Extended basis coverage volumes



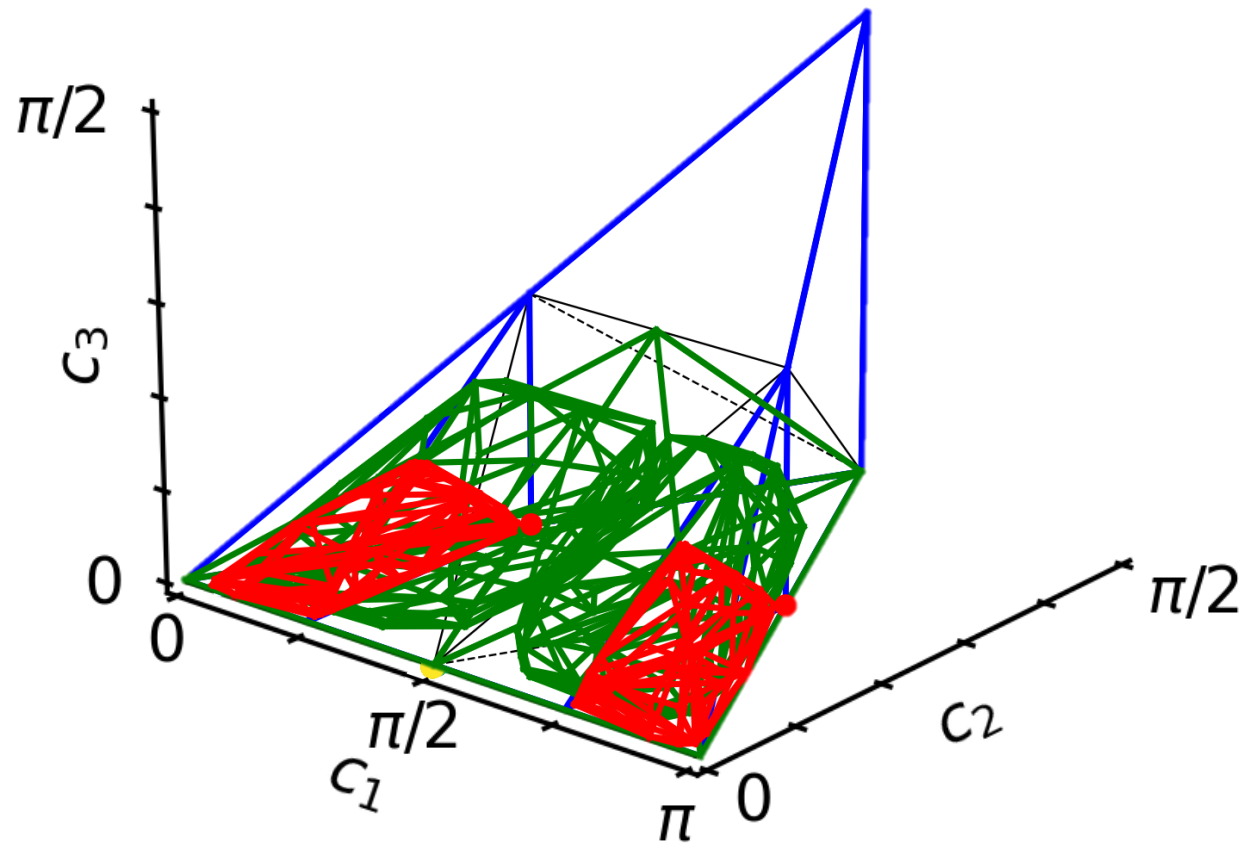
➤ Single gates have non-zero volume!

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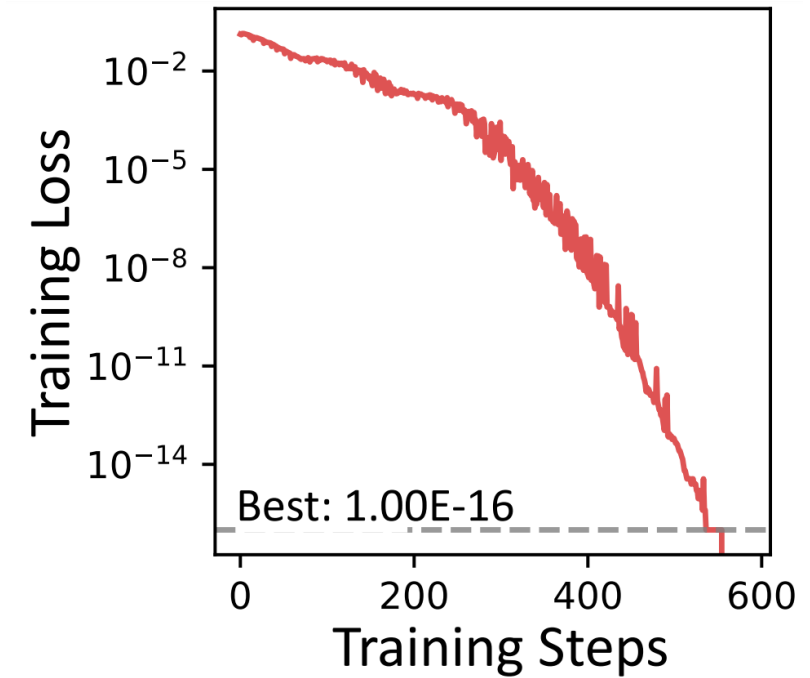
Target\Basis	$\sqrt{i\text{SWAP}}$	PD + $\sqrt{i\text{SWAP}}$
CNOT	1.75	1.5
SWAP	2.5	2.25
Haar	1.9	1.7

Extended basis coverage volumes



➤ Single gates have non-zero volume!

➤ Nelder-Mead optimization over Makhlin invariants functional

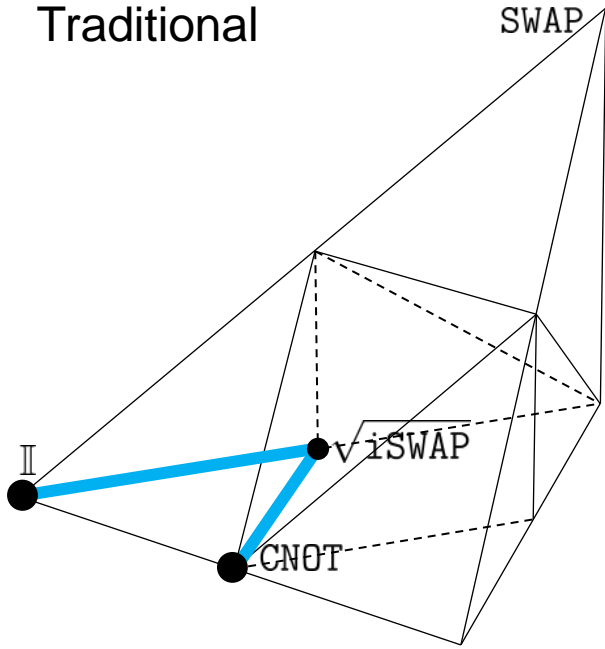


Target/Basis	$\sqrt{i\text{SWAP}}$	PD + $\sqrt{i\text{SWAP}}$
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Cartan trajectories for \sqrt{i} SWAP

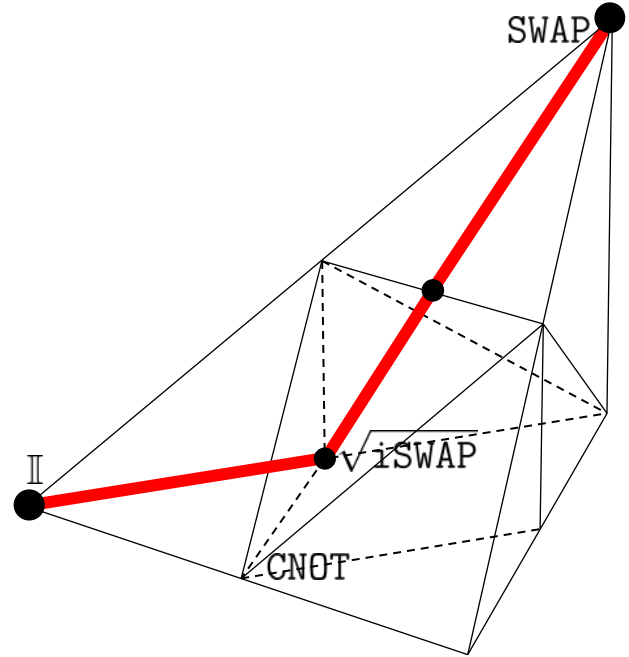
Traditional

SWAP



SWAP

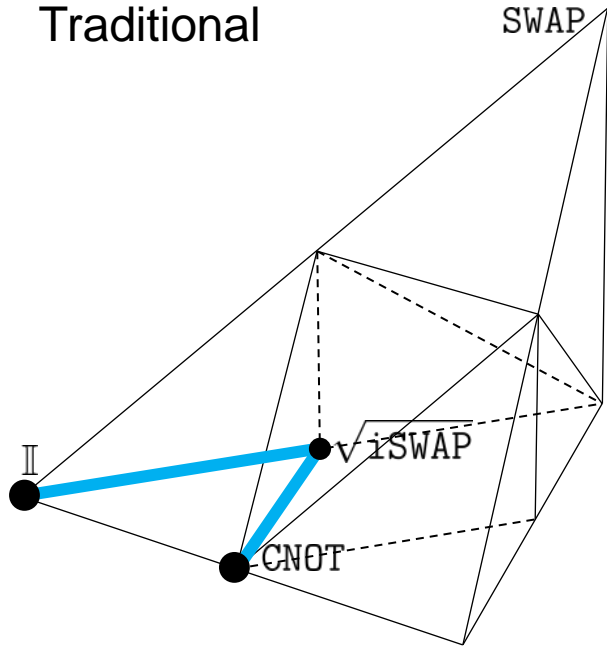
● 1Q Gates



Cartan trajectories for \sqrt{i} SWAP

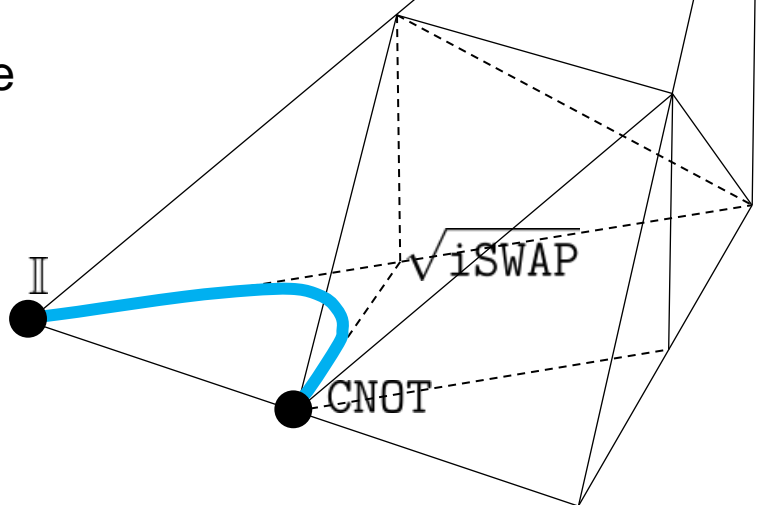
Traditional

SWAP



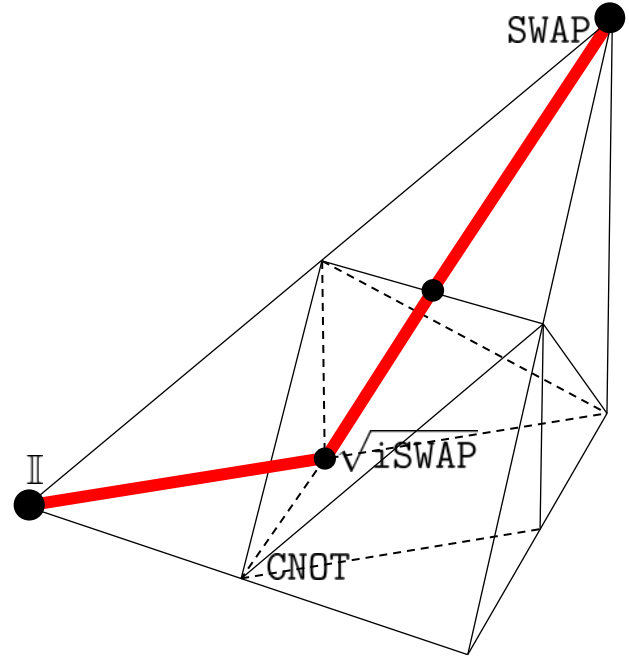
SWAP

Parallel-Drive
Optimized

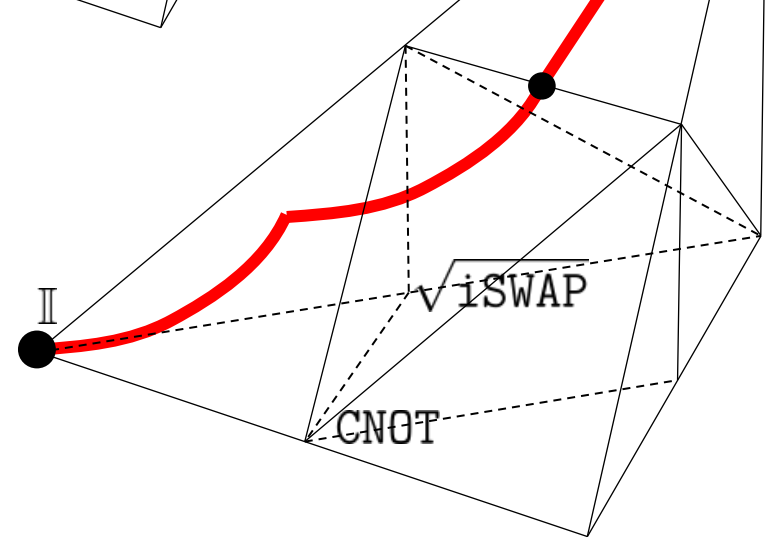


SWAP

● 1Q Gates

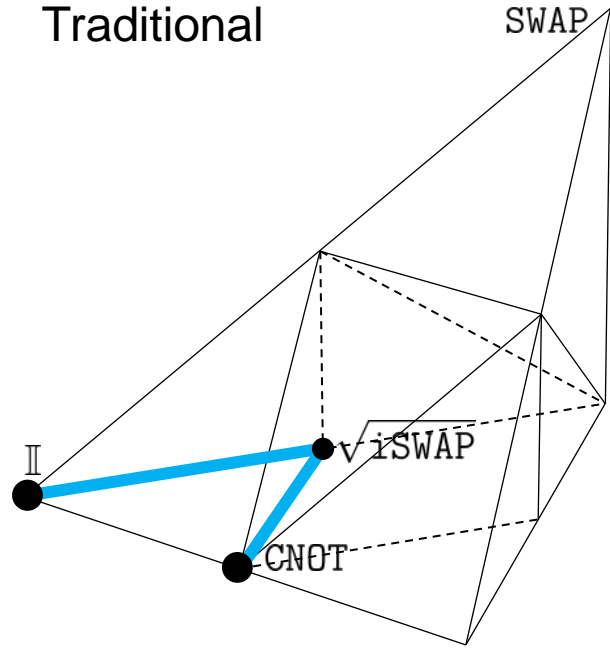


SWAP

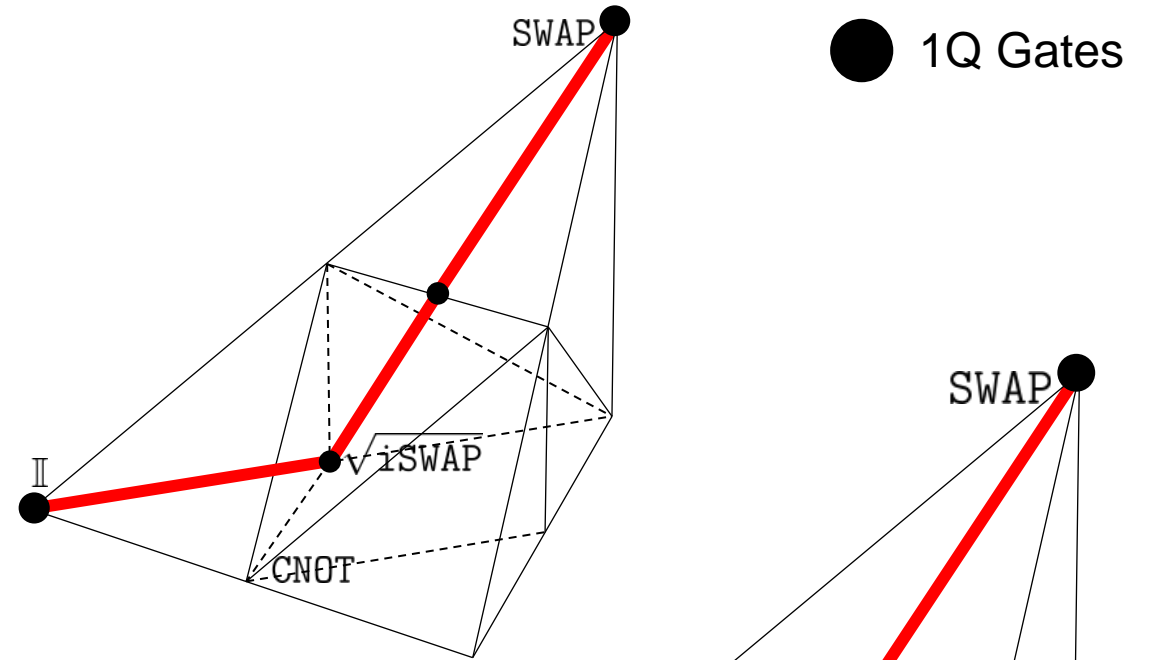
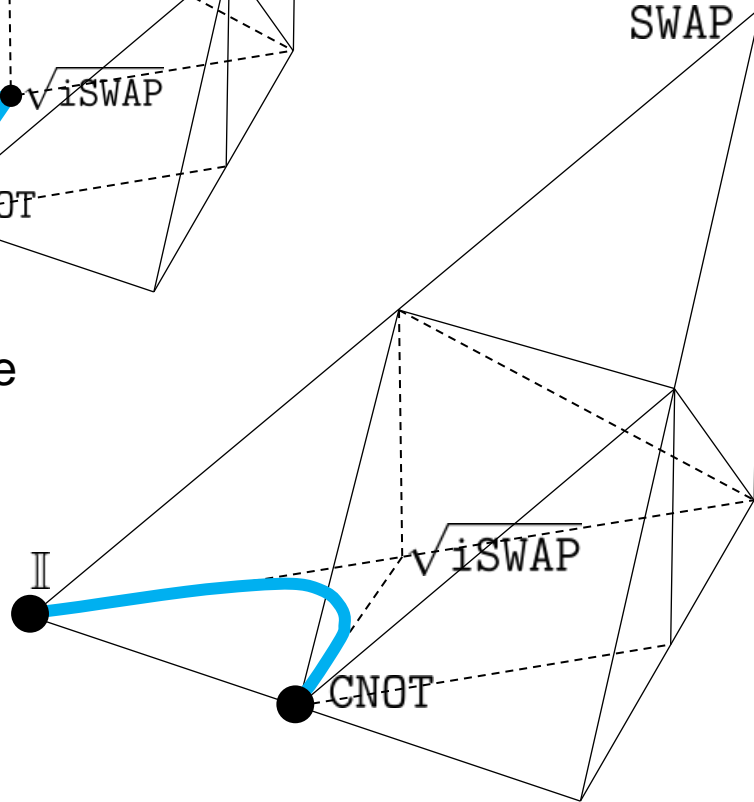


Cartan trajectories for \sqrt{i} SWAP

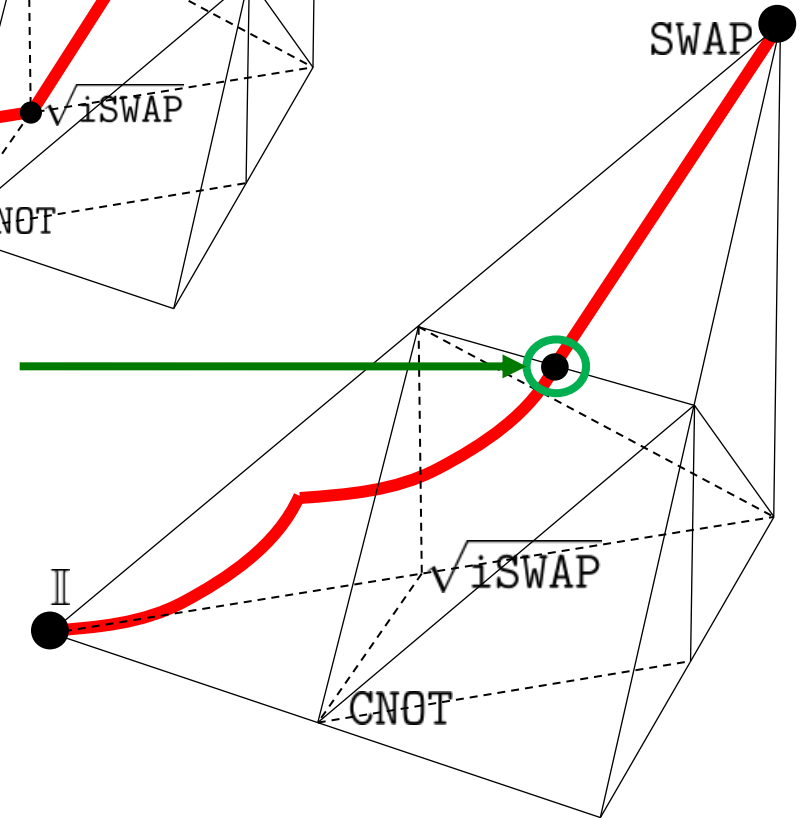
Traditional



Parallel-Drive Optimized



Removable

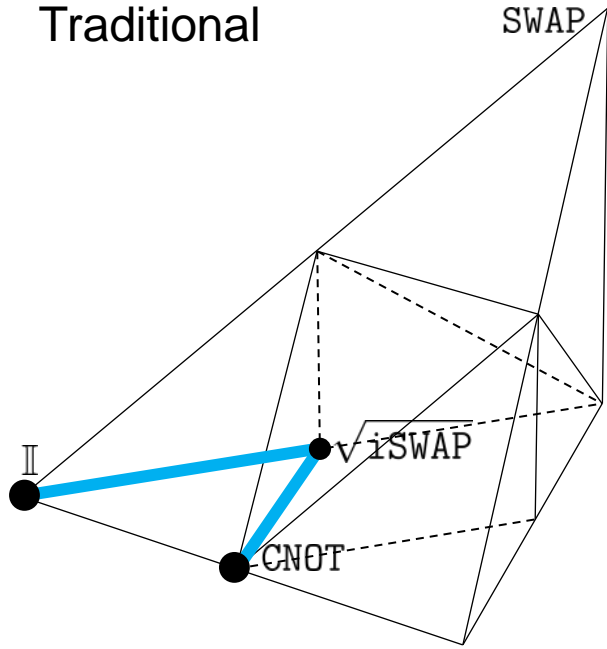


● 1Q Gates

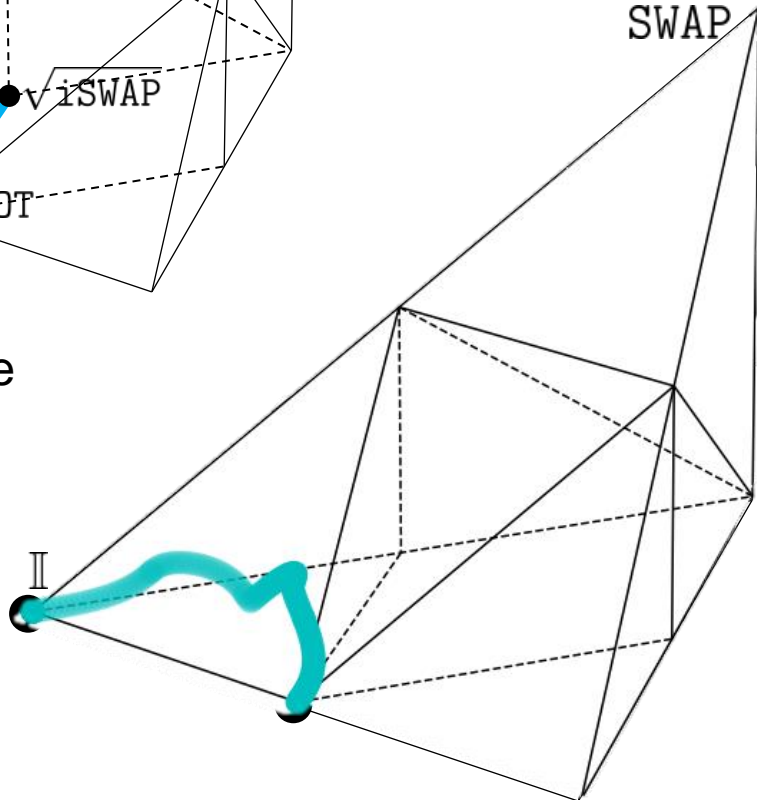
Cartan trajectories for \sqrt{i} SWAP

Traditional

SWAP



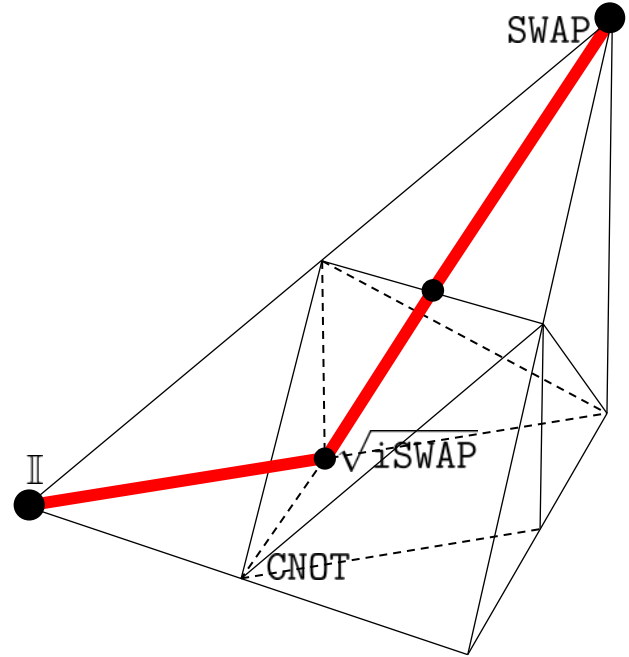
SWAP



Parallel-Drive
Optimized

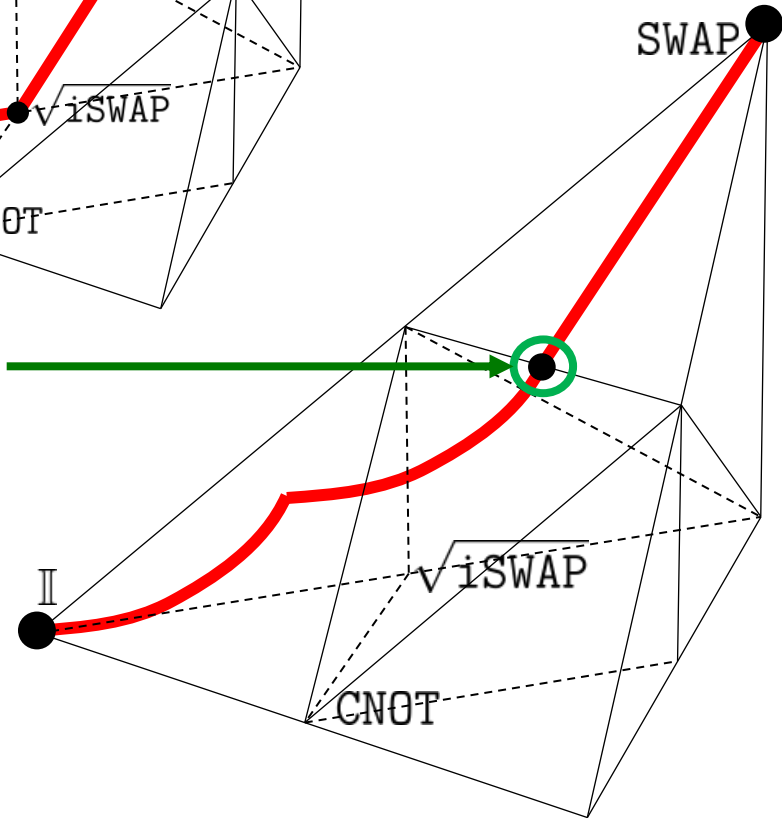
SWAP

● 1Q Gates



Removable

SWAP



Conclusion

1. Decrease circuit duration by 17.84% over NISQ benchmarks!
2. Improve fidelity using \sqrt{i} SWAP basis by 10.5% for random gates
3. Next steps, hardware realization

McKinney, et al. **ISCA** (2023)

