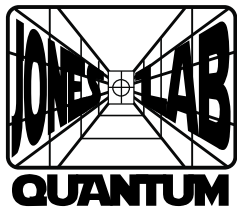


Co-designed architectures for modular superconducting quantum computers

Evan McKinney[†],
M. Hatridge[§], A.K. Jones[†]



[†]Department of Electrical and Computer Engineering, University of Pittsburgh
[§]Department of Applied Physics, Yale University

YQI, September 2024

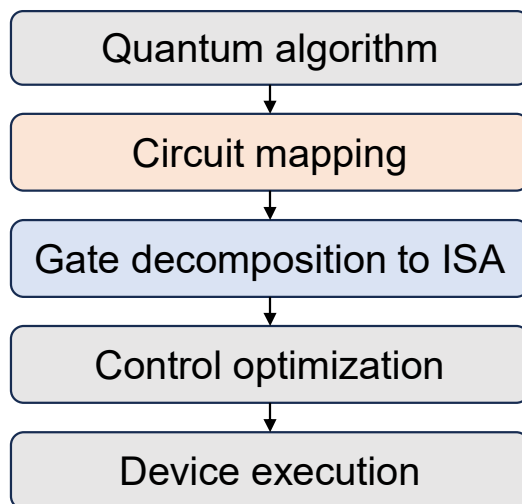


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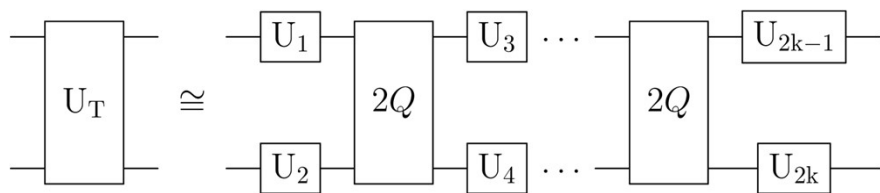
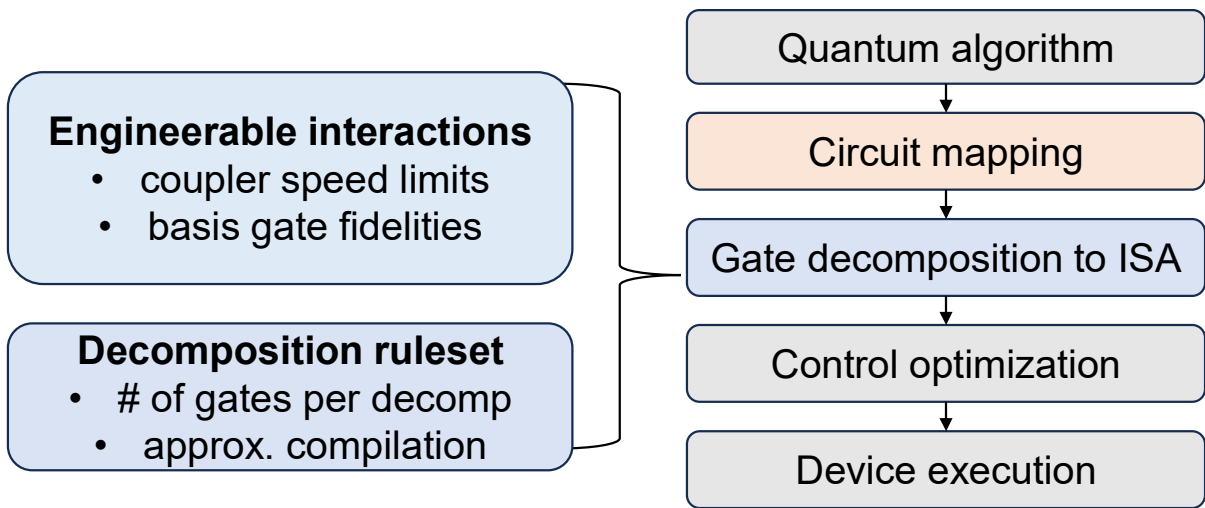




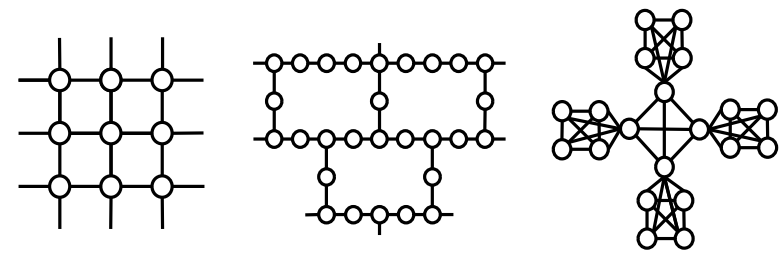
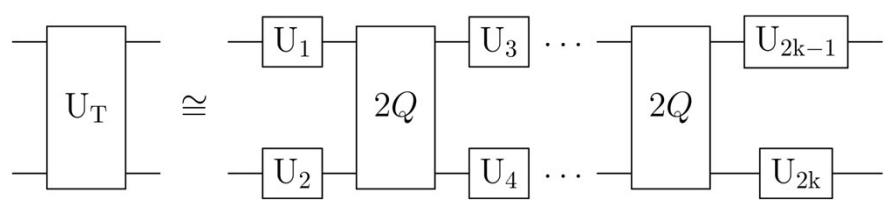
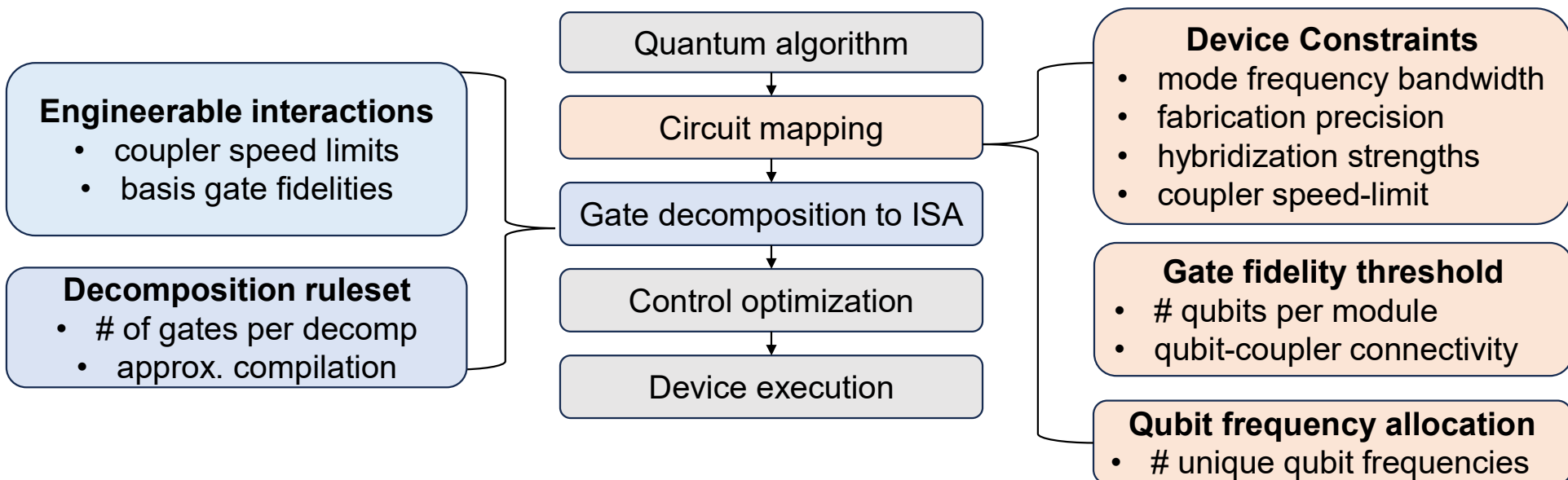
Transpilation as co-design framework



Transpilation as co-design framework

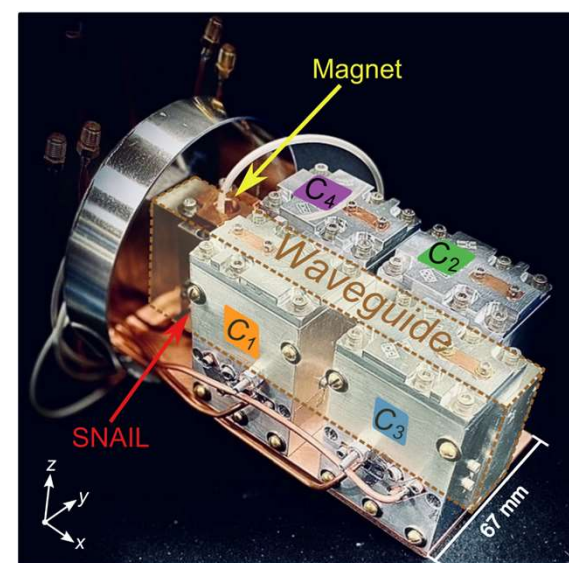
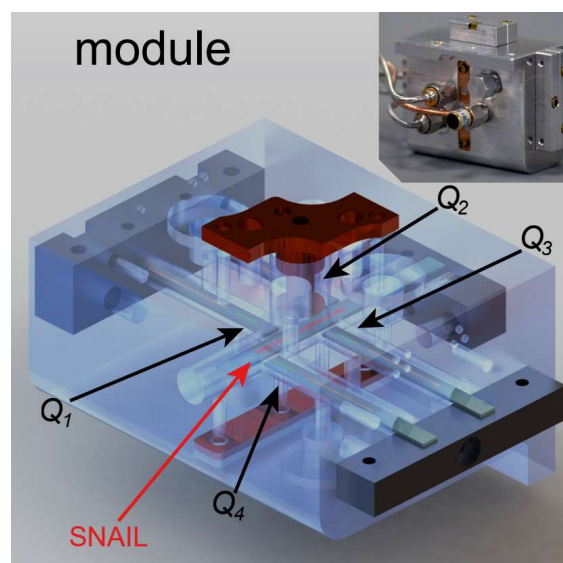
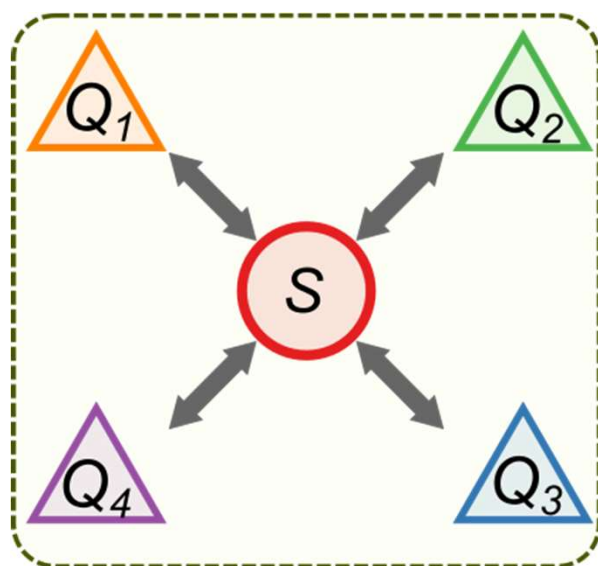


Transpilation as co-design framework



SNAIL module

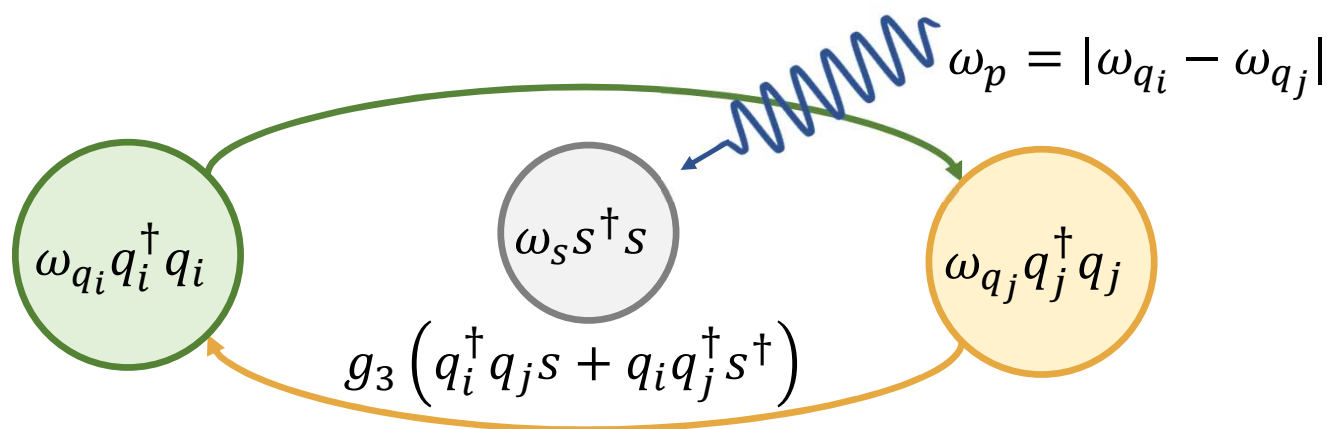
Four qubit SNAIL-based quantum module



Xia, et al. [arXiv:2306.10162](https://arxiv.org/abs/2306.10162) (2023)

Zhou, et al. *npj Quantum Inf* **9**, 54 (2023)

Parametric two qubit gates



$$\frac{H_{eff}}{\hbar} = g_2^{eff} (a^\dagger b + ab^\dagger), \quad \text{where } g_2^{eff} = g_3 \left(\frac{g}{\Delta}\right)^2 \sqrt{n_p}$$

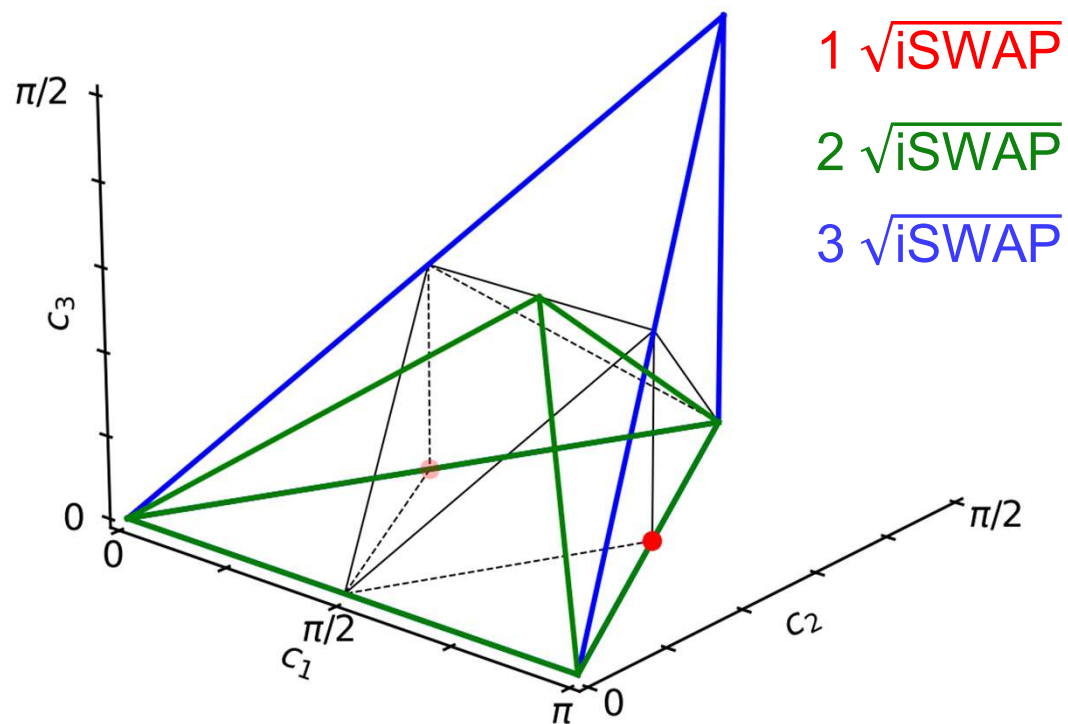
Clerk, et al. **Reviews of Modern Physics** (2010)

Bergeal, et al. **Nature Physics** (2010)

Frattini, et al. **Applied Physics Letters** (2017)

Efficient instruction sets using \sqrt{i} SWAP

$$\sqrt{i}\text{SWAP} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & \frac{1}{\sqrt{2}} & \frac{i}{\sqrt{2}} & 0 \\ 0 & \frac{i}{\sqrt{2}} & \frac{1}{\sqrt{2}} & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

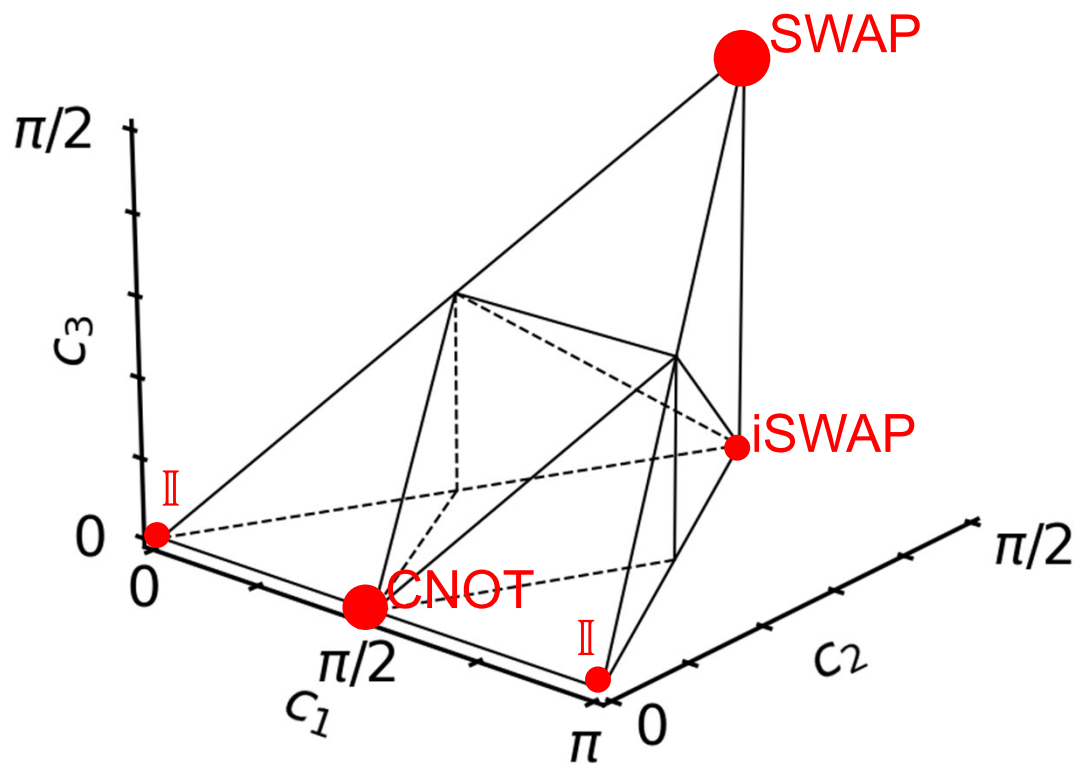
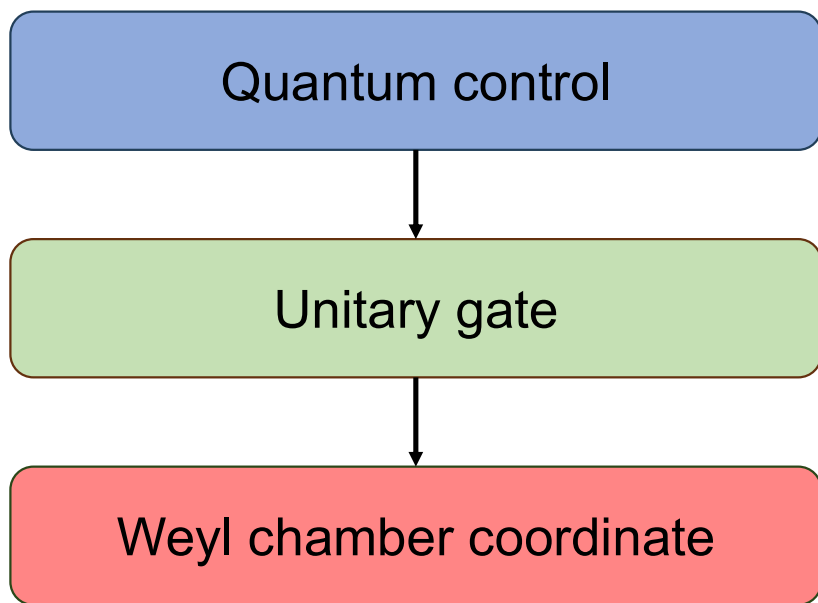


McKinney, et al. **ISCA** (2023)

Huang, et al. **Physical Review Letters** (2023)

Chen, et al. **arxiv:2312.05652** (2023)

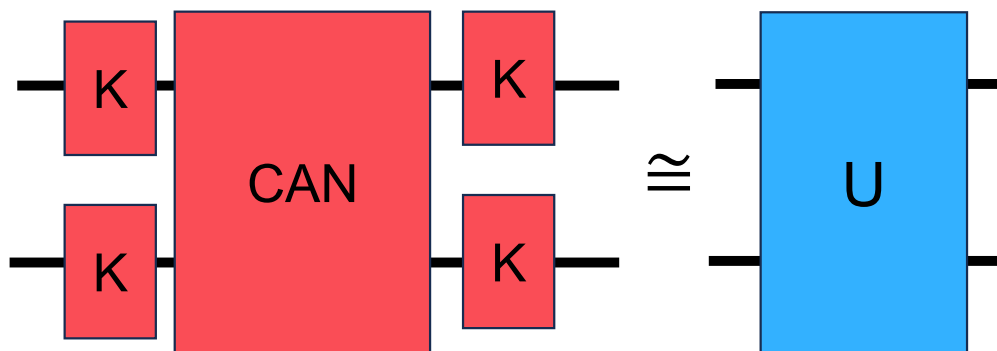
Geometrically representing quantum gates



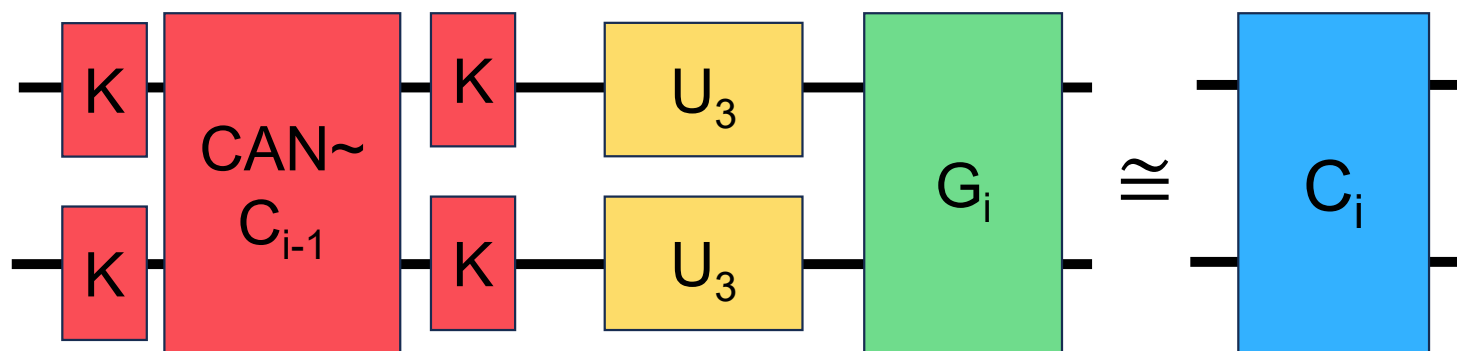
Peterson, et al. **Quantum** 4 (2020)
 Makhlin, Yuriy. **Quantum Information Processing** (2002)
 Watts, et al. **Entropy** 15 (2013)
 Zhang, et al. **Physical Review A** (2003)

Cartan KAK decomposition

All 2Q gates can be specified by 3 invariants up to local rotations (1Q)



$$U = (K_1 \otimes K_2) e^{-i(k_x \sigma_{XX} + k_y \sigma_{YY} + k_z \sigma_{ZZ})} (K_3 \otimes K_4)$$





Conversion/Gain candidate basis gates



- Engineerable interactions from 3-wave mixing

$$\hat{H} = g_c(e^{i\phi_c} a^\dagger b + e^{-i\phi_c} a b^\dagger) + g_g(e^{i\phi_g} a b + e^{-i\phi_g} a^\dagger b^\dagger)$$

- Native gates limited to XX,YY components

$$\hat{H} = \frac{1}{2}[(g_c + g_g)XX + (g_c - g_g)YY]$$

- Cartan trajectories from Makhlin invariants

$$G_1 = (\cos(2g_c t) + \cos(2g_g t))^2 / 4$$

$$G_2 = \cos(2(g_c - g_g)t) + \cos(2(g_c + g_g)t) + 1$$



Conversion/Gain candidate basis gates



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$$\hat{H} = g_c(e^{i\phi_c} a^\dagger b + e^{-i\phi_c} ab^\dagger) + g_g(e^{i\phi_g} ab + e^{-i\phi_g} a^\dagger b^\dagger)$$

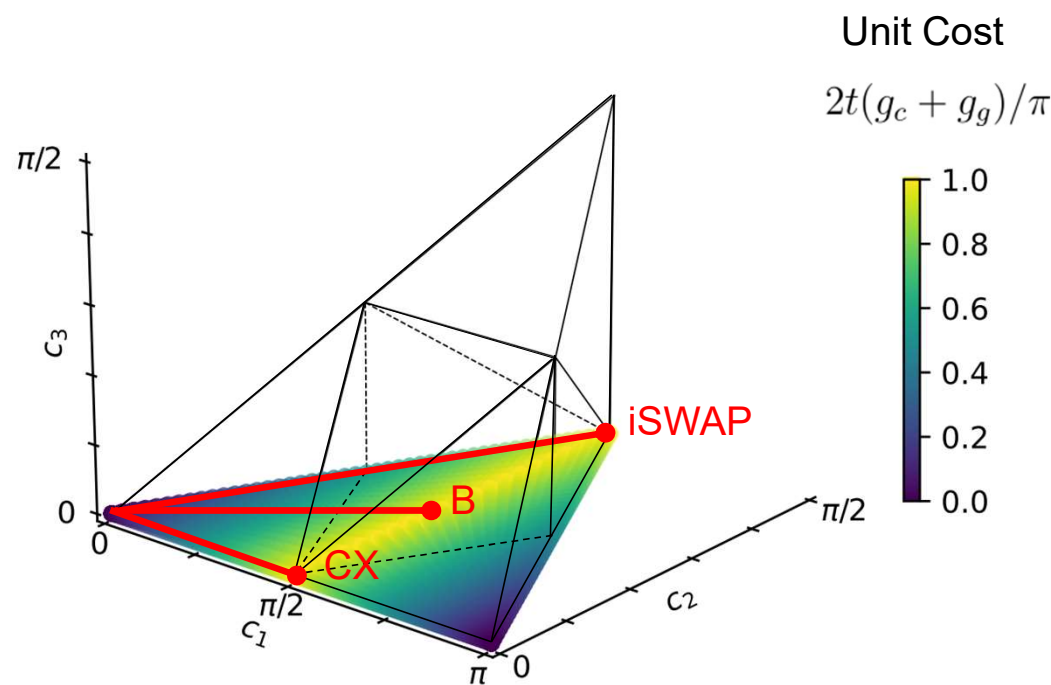
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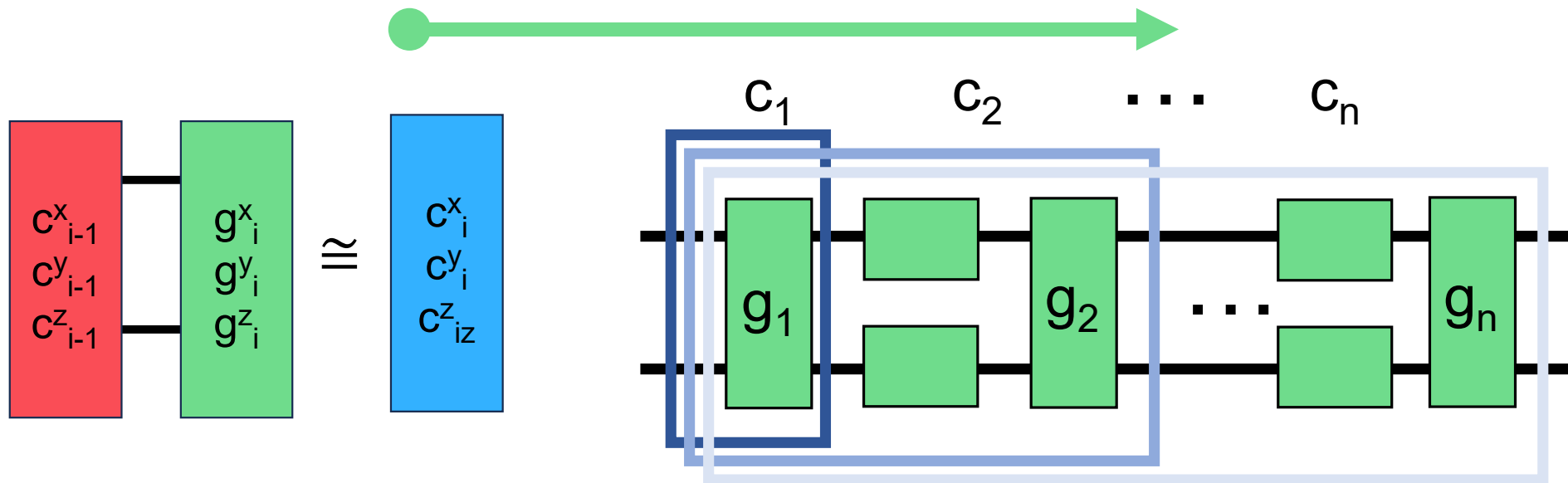
Monodromy polytopes

Satisfying all 72 quantum Littlewood-Richardson linear inequalities implies

given a circuit with invariant \mathbf{c}_{i-1} ,

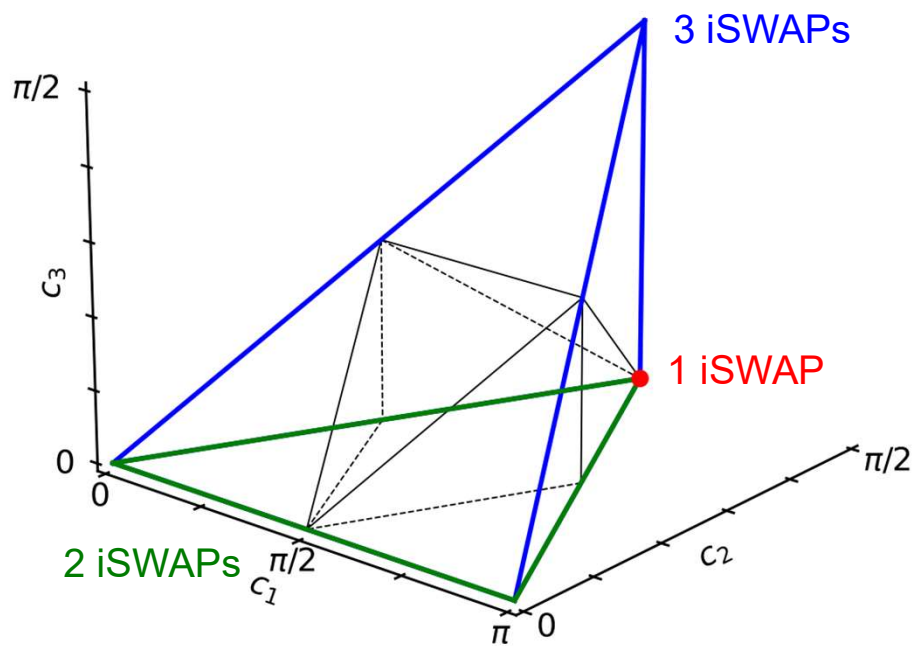
appending g_i , a gate from the device's instruction set,

can yield a circuit with invariant \mathbf{c}_i .



Satisfy all $L_i(\mathbf{c}_{i-1}, g_i, \mathbf{c}_i)$ such that $\forall i, g_i \in \text{ISA}$

Basis coverage volumes

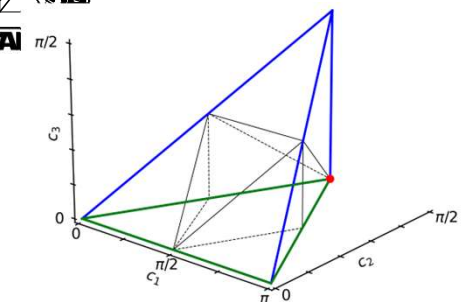


➤ **Monodromy polytopes** finds minimum gate applications for any 2Q target gate!

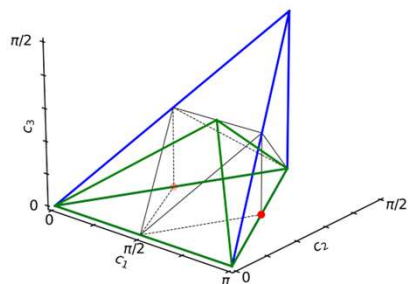
Target\Basis	iSWAP
CNOT	2.0
SWAP	3.0
Haar	3.0

Peterson, et al. *Quantum* 4 (2020)
 McKinney, et al. *ISCA* (2023)

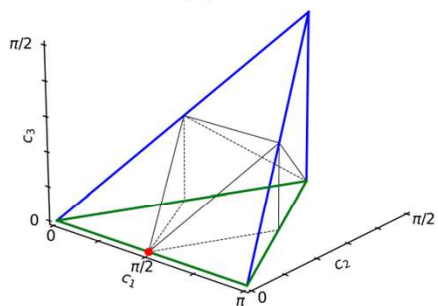
Basis coverage volumes



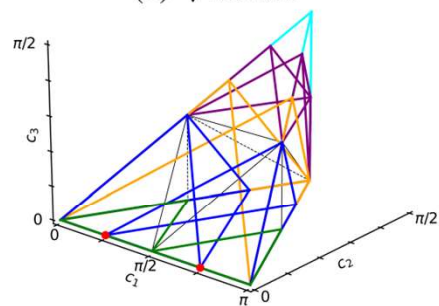
(a) iSWAP



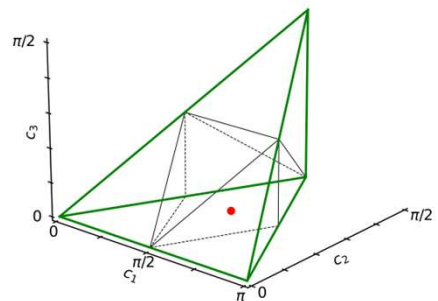
(b) $\sqrt{i\text{SWAP}}$



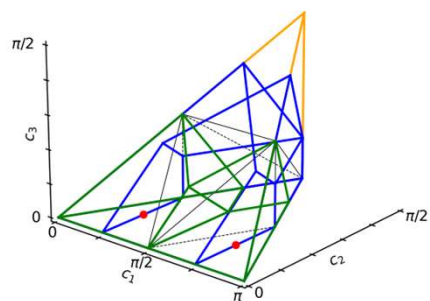
(c) CNOT



(d) $\sqrt{\text{CNOT}}$



(e) B



(f) \sqrt{B}

➤ **Monodromy polytopes** finds minimum gate applications for any 2Q target gate!

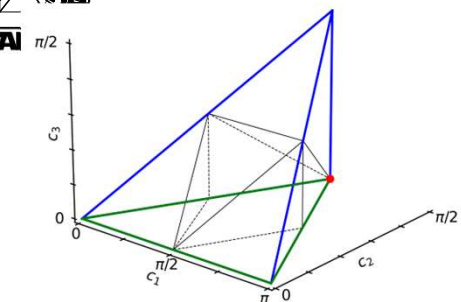
Decomposition *gate count* costs

Target\Basis	iSWAP	$\sqrt{i\text{SWAP}}$	CX	$\sqrt{\text{CX}}$	B	\sqrt{B}
CNOT	2.0	2.0	1.0	2.0	2.0	2.0
SWAP	3.0	3.0	3.0	6.0	2.0	4.0
Haar	3.0	2.2	3.0	3.5	2.0	3.1

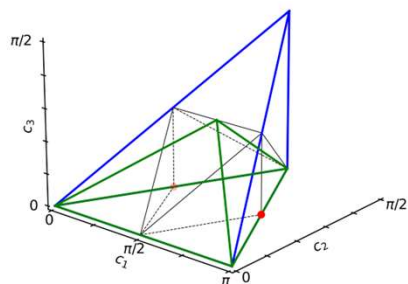
Peterson, et al. *Quantum* 4 (2020)

McKinney, et al. *ISCA* (2023)

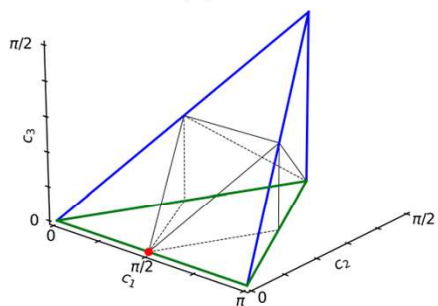
Basis coverage volumes



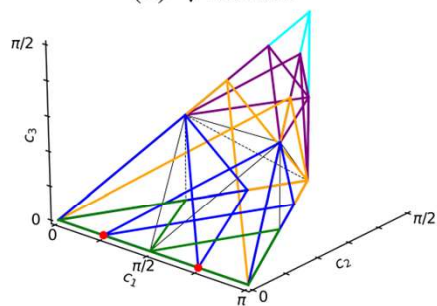
(a) iSWAP



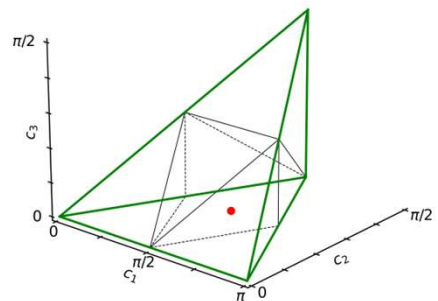
(b) $\sqrt{i\text{SWAP}}$



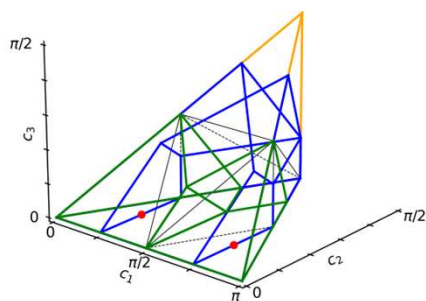
(c) CNOT



(d) $\sqrt{\text{CNOT}}$



(e) B



(f) \sqrt{B}

➤ **Monodromy polytopes** finds minimum gate applications for any 2Q target gate!

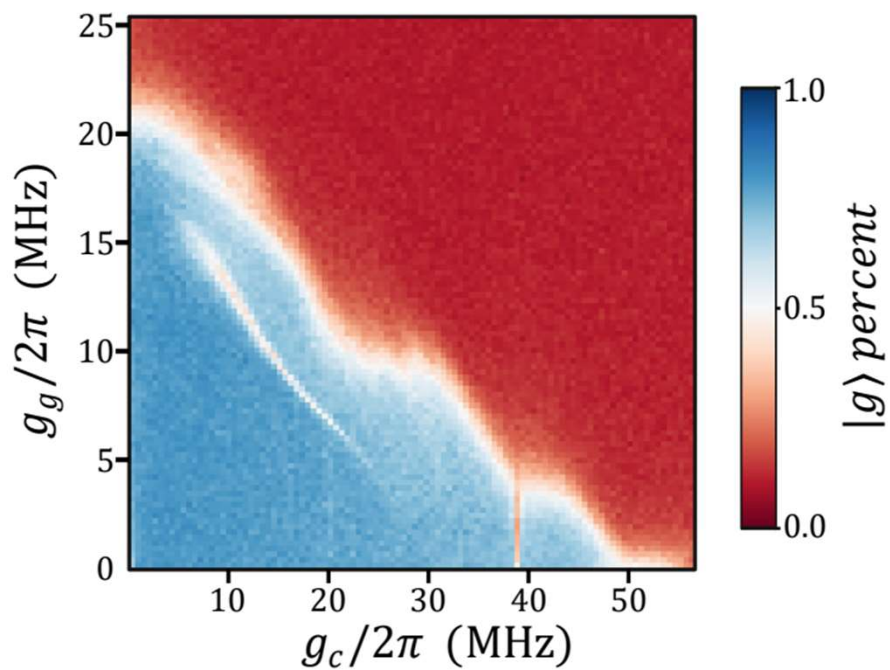
Decomposition *gate count* costs

Target\Basis	iSWAP	$\sqrt{i\text{SWAP}}$	CX	$\sqrt{\text{CX}}$	B	\sqrt{B}
CNOT	2.0	2.0	1.0	2.0	2.0	2.0
SWAP	3.0	3.0	3.0	6.0	2.0	4.0
Haar	3.0	2.2	3.0	3.5	2.0	3.1

Peterson, et al. *Quantum* 4 (2020)

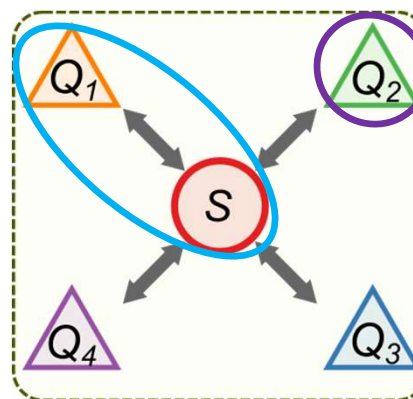
McKinney, et al. *ISCA* (2023)

Hardware speed limits



Limitation of SNAIL when driving both gain and conversion

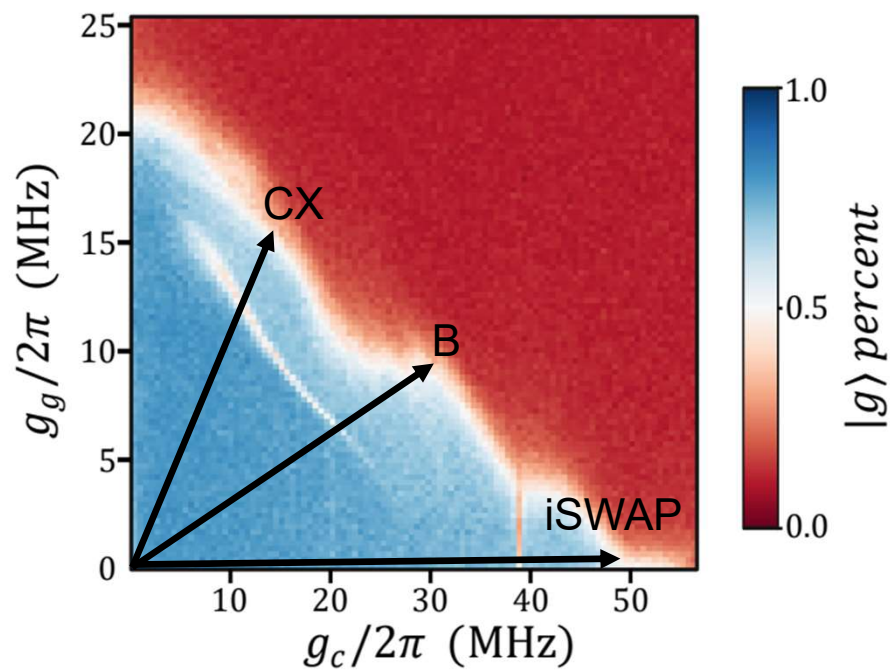
Module



Drives applied between SNAIL and qubit

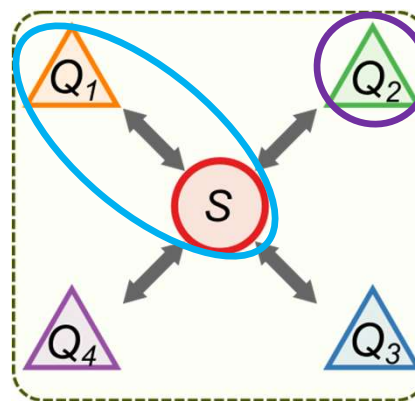
Measure second qubit to witness SNAIL breakpoint

Hardware speed limits



Limitation of SNAIL when driving both gain and conversion

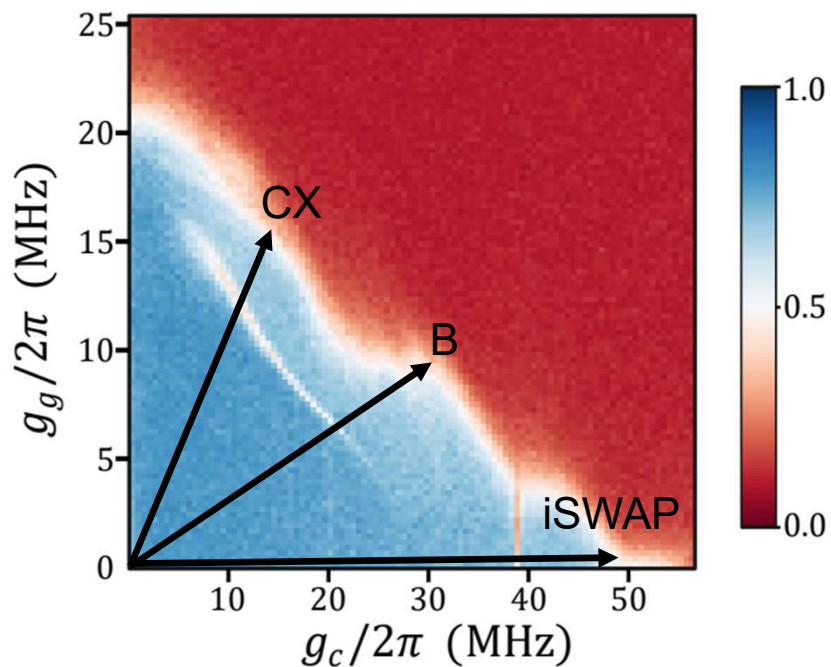
Module



Drives applied between SNAIL and qubit

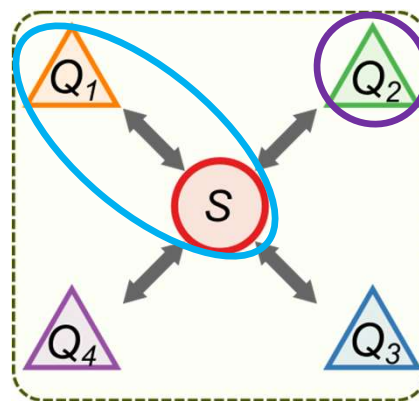
Measure second qubit to witness SNAIL breakpoint

Hardware speed limits



Limitation of SNAIL when driving both gain and conversion

Module



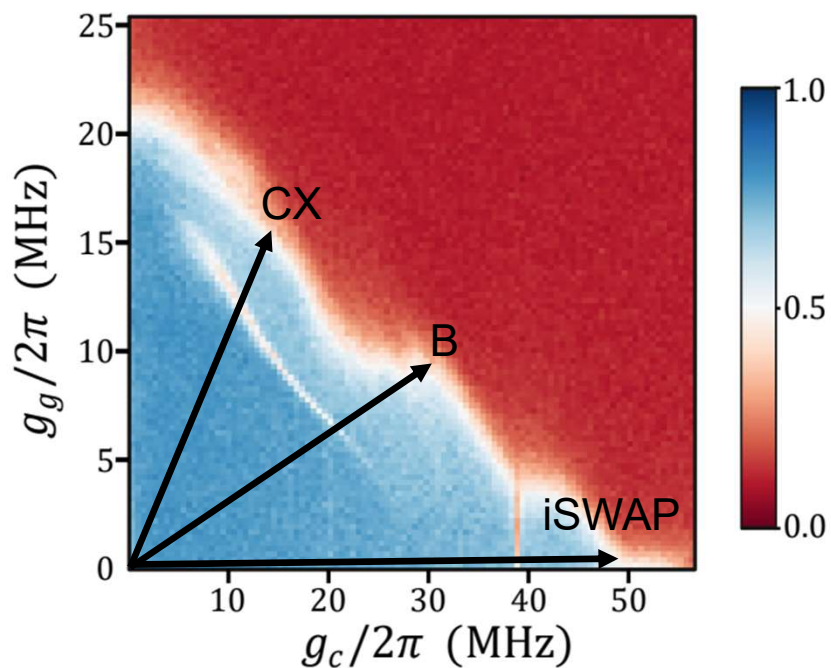
Drives applied between SNAIL and qubit

Measure second qubit to witness SNAIL breakpoint

Decomposition normalized *duration* costs

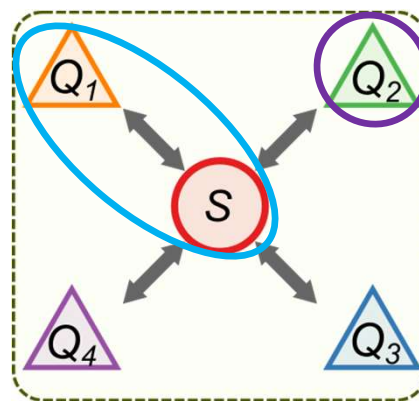
Target\Basis	iSWAP	\sqrt{iSWAP}	CX	\sqrt{CX}	B	\sqrt{B}
Duration	1.0	0.5	1.8	0.9	1.4	0.7
CNOT	2.0	1.0	1.8	1.8	2.8	1.4
SWAP	3.0	1.5	5.4	5.4	2.8	2.8
Haar	3.0	1.1	5.4	3.2	2.8	2.2

Hardware speed limits



Limitation of SNAIL when driving both gain and conversion

Module



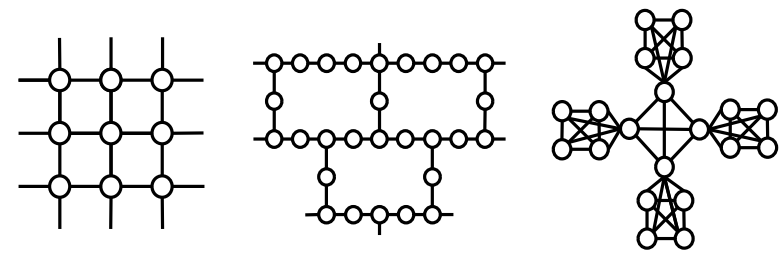
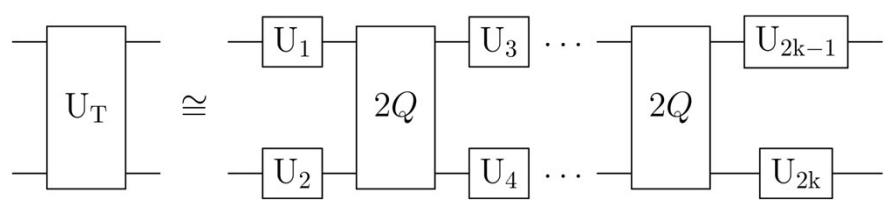
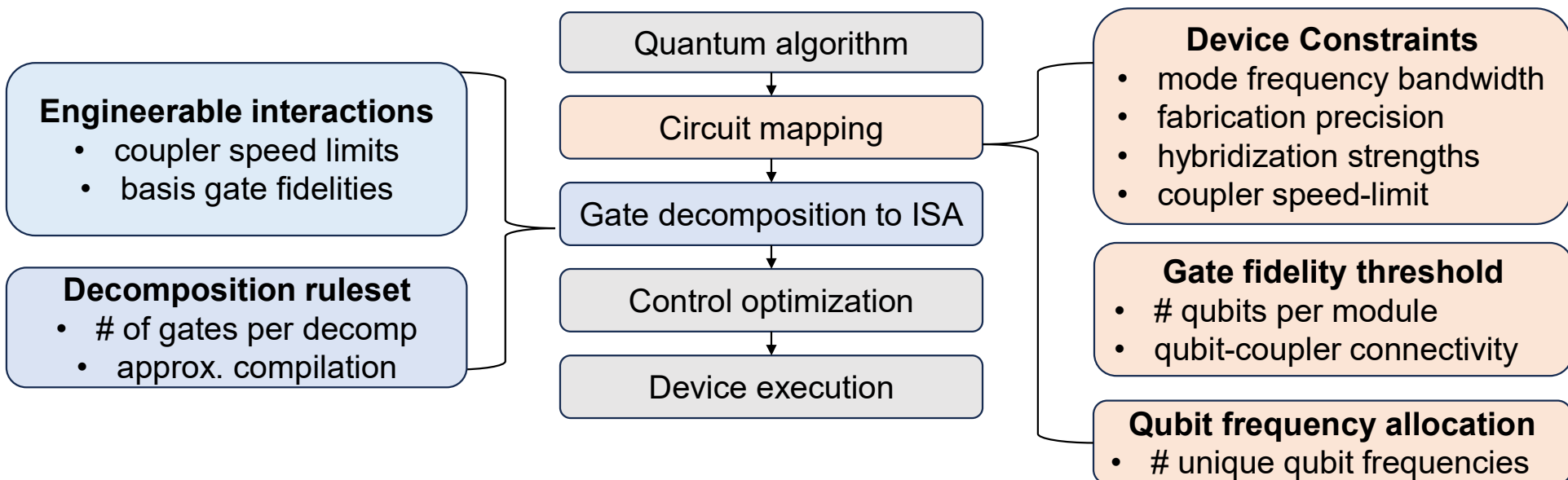
Drives applied between SNAIL and qubit

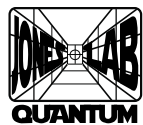
Measure second qubit to witness SNAIL breakpoint

Decomposition normalized *duration* costs

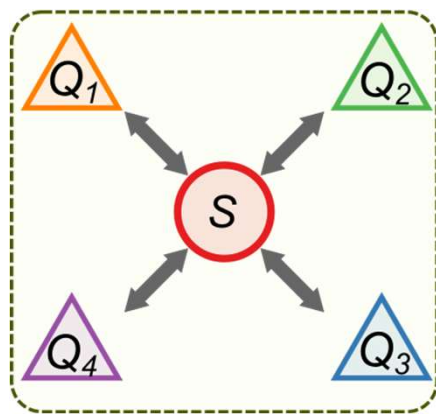
Target\Basis	iSWAP	\sqrt{iSWAP}	CX	\sqrt{CX}	B	\sqrt{B}
Duration	1.0	0.5	1.8	0.9	1.4	0.7
CNOT	2.0	1.0	1.8	1.8	2.8	1.4
SWAP	3.0	1.5	5.4	5.4	2.8	2.8
Haar	3.0	1.1	5.4	3.2	2.8	2.2

Transpilation as co-design framework

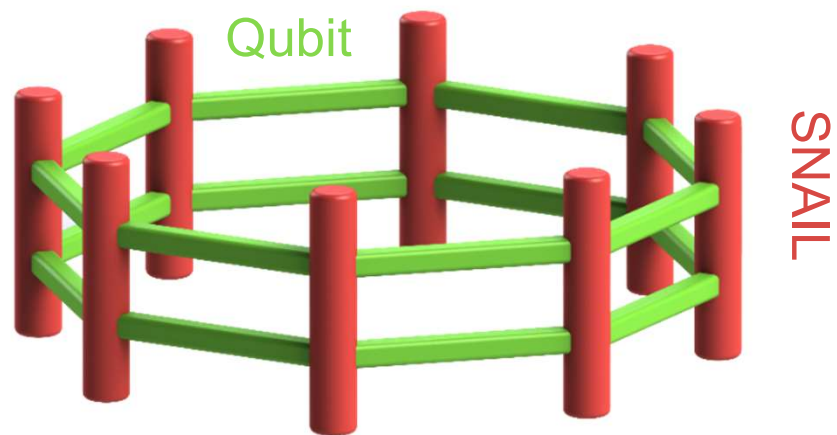
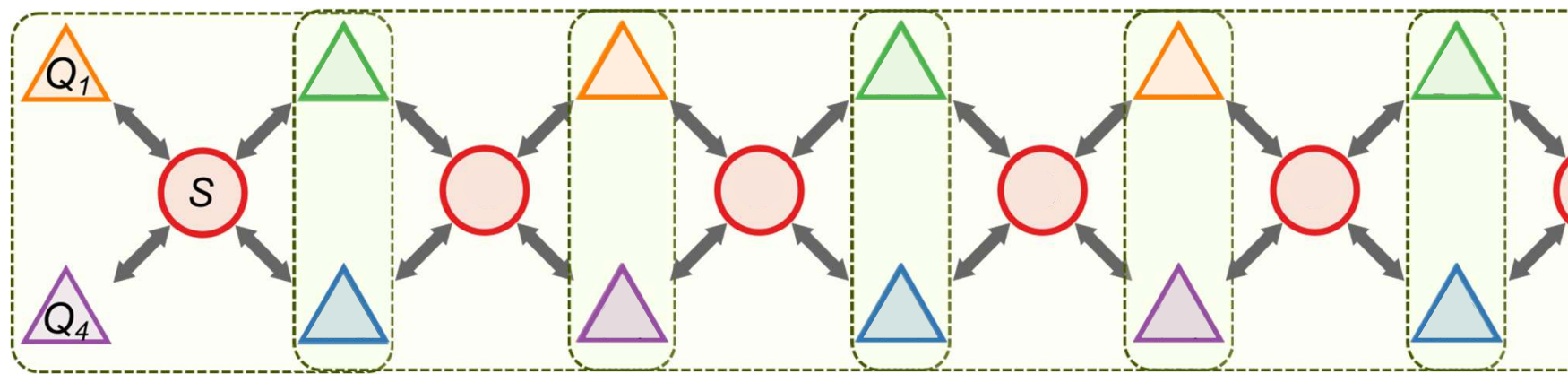




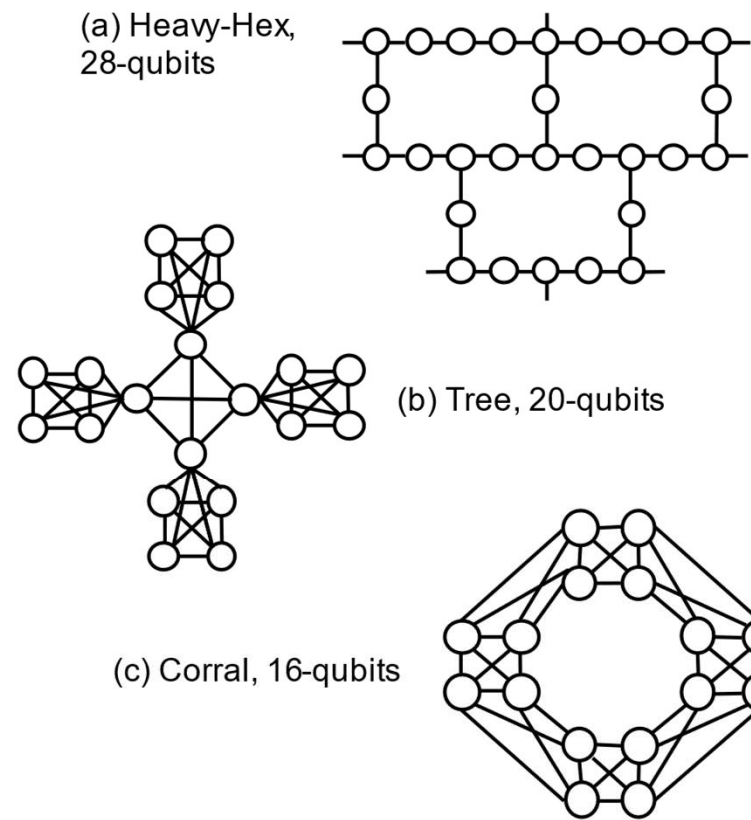
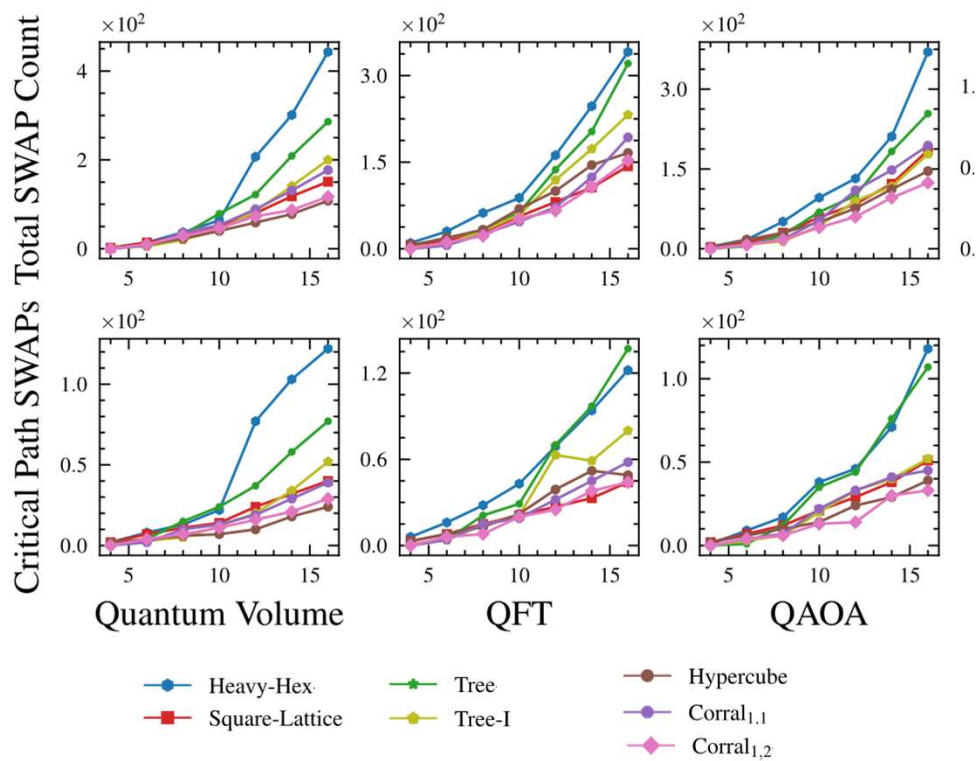
Extending the module



Extending the module

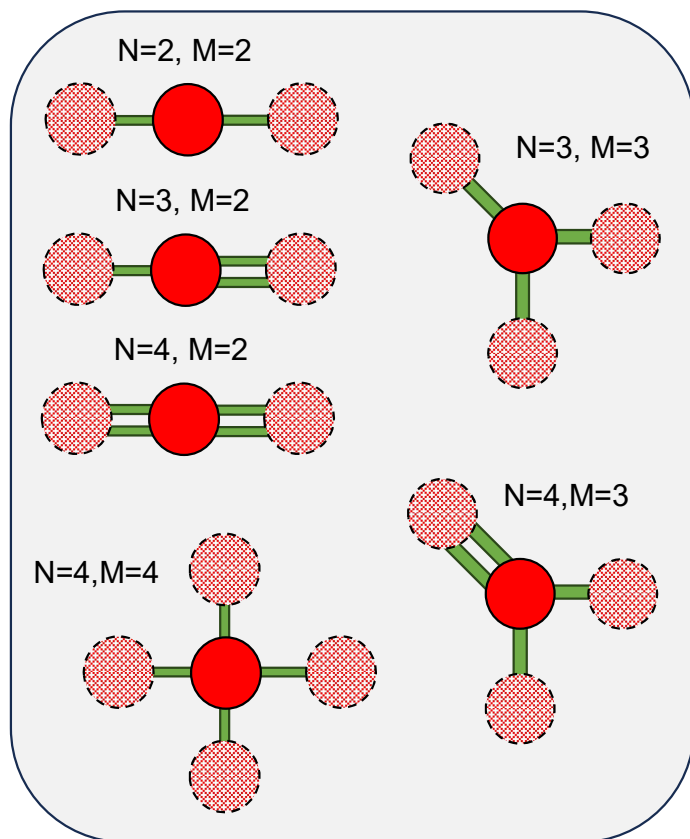


Connectivity reduces circuit costs

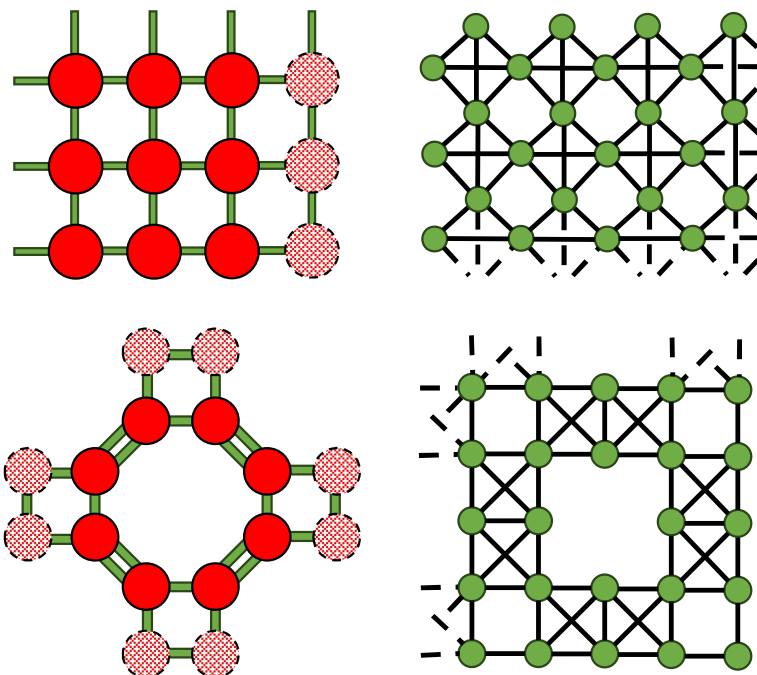


Alternative designs?

SNAIL and qubit frequencies **must yield unique sets of parametric drives** per neighborhoods

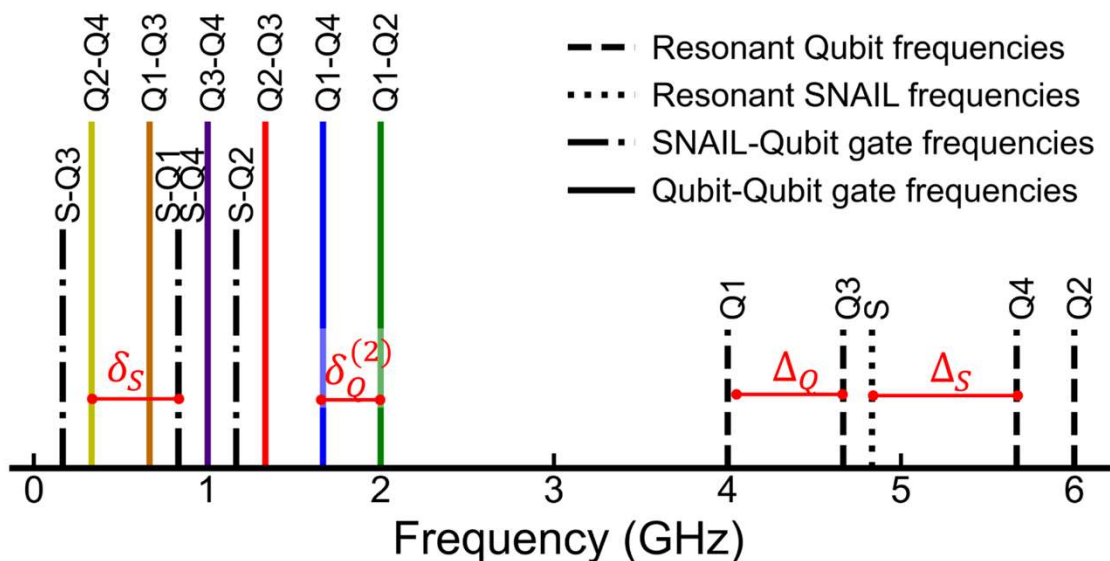


Maximum incident edges per node (N)?
 Maximum adjacent vertices (M)?
 Maximum vertex variants (k)?



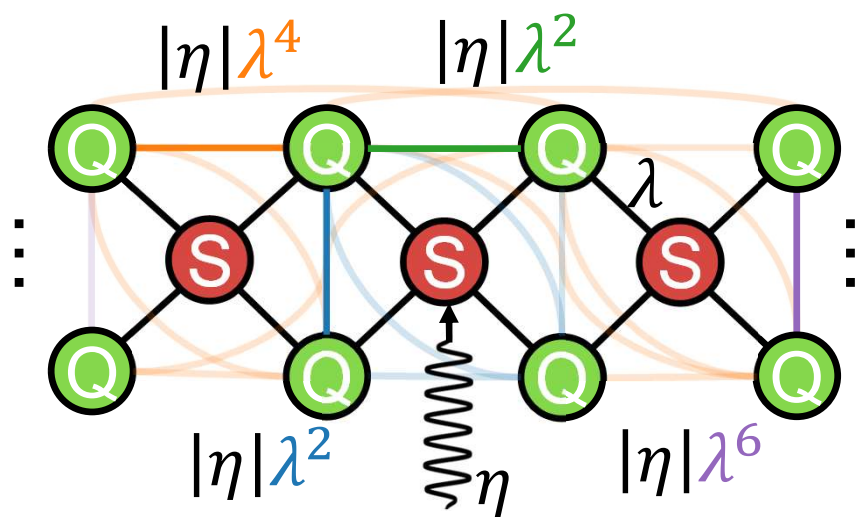
Spectral crowding of terms

$$\tilde{H}_I = g_3 \left(se^{-i\tilde{\omega}_s t} + \eta e^{-i\omega_p t} + \sum_i \lambda_{si} q_i e^{-i\tilde{\omega}_{q_i} t} + \text{h.c.} \right)^3 + \sum_i \frac{\alpha_i}{12} \left(q_i e^{-i\tilde{\omega}_{q_i} t} - \lambda_{si} (se^{-i\tilde{\omega}_s t} + \eta e^{-i\omega_p t}) + \text{h.c.} \right)^4$$



Spectator error budgeting

- Intra-module terms protected by frequency separation
- Inter-module terms protected by weak SNAIL-SNAIL hybridization



$$\eta = (\epsilon^x + i\epsilon^y) \frac{\omega_s}{(\omega_p^2 - \omega_s^2)}$$

$$H_{conv} = \sum_{i>j} q_i^\dagger q_j \left(6\eta g_3 \lambda^2 e^{-it(\omega_{q_i} - \omega_{q_j} + \omega_p)} \right) + \text{h.c.}$$

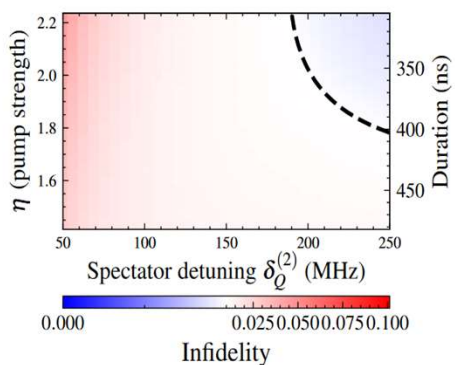
$$H(t) = 6|\eta|g_3\lambda^2 \left(\mathbf{q}_1^\dagger \mathbf{q}_2 + \frac{2}{\delta_Q^{(2)} \log 2} \mathbf{q}_3^\dagger \mathbf{q}_4 \right)$$

When is RWA a good approximation?

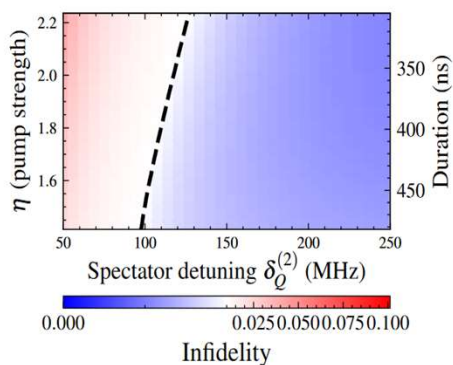
Error budget as a separation design constraint

$$F_{\text{avg}}(U, V) = \frac{16 \text{Tr}[UV^\dagger] + 1}{17} \quad \text{Threshold at } F > .99$$

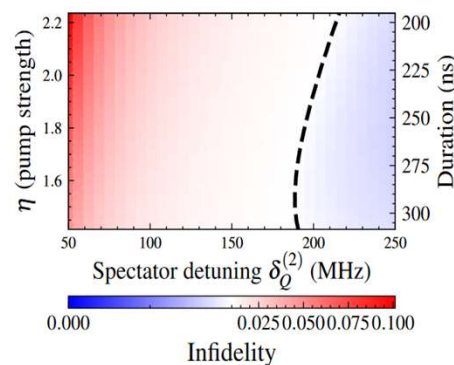
iSWAP



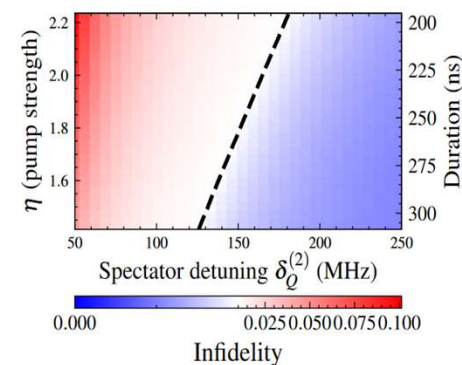
(a) $\lambda = 0.08, T_1 = 80 \mu\text{s}$



(b) $\lambda = 0.08, T_1 = 160 \mu\text{s}$

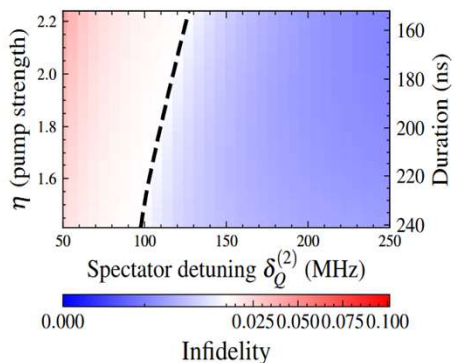


(c) $\lambda = 0.1, T_1 = 80 \mu\text{s}$

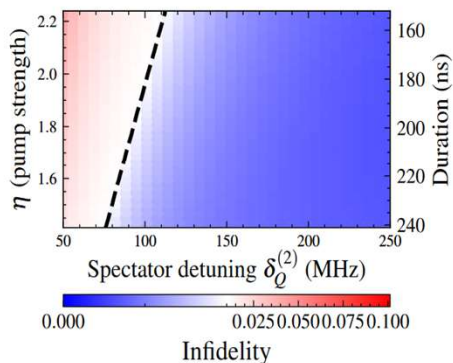


(d) $\lambda = 0.1, T_1 = 160 \mu\text{s}$

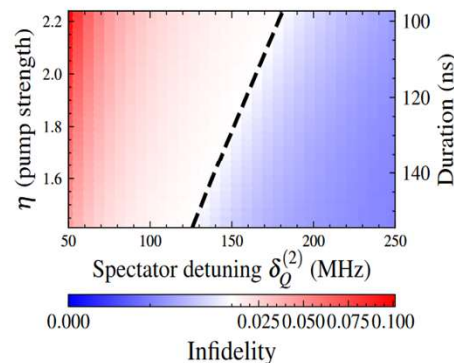
√iSWAP



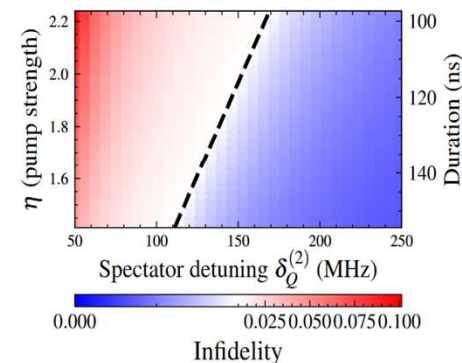
(e) $\lambda = 0.08, T_1 = 80 \mu\text{s}$



(f) $\lambda = 0.08, T_1 = 160 \mu\text{s}$

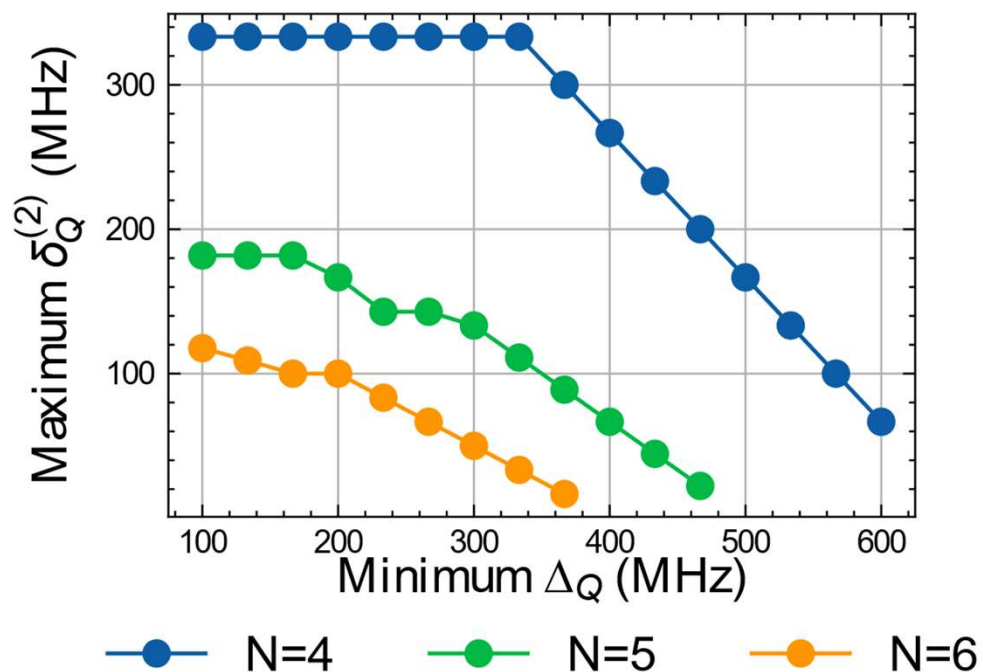


(g) $\lambda = 0.1, T_1 = 80 \mu\text{s}$



(h) $\lambda = 0.1, T_1 = 160 \mu\text{s}$

Satisfying constraints using linear programming



➤ Binary search:
 maximum conversion separation (y-axis)
 given minimum qubit separation (x-axis)

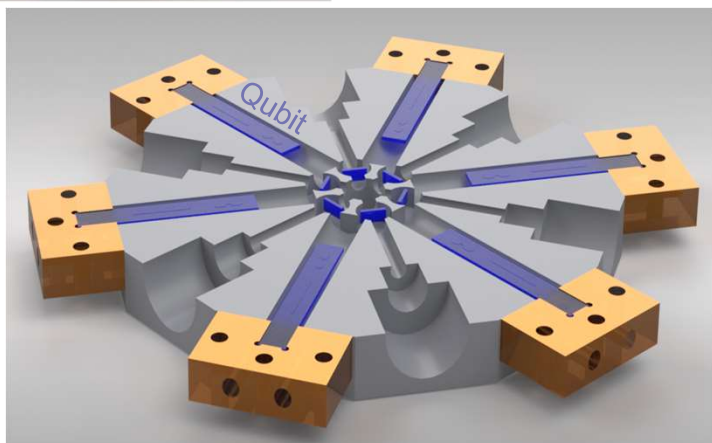
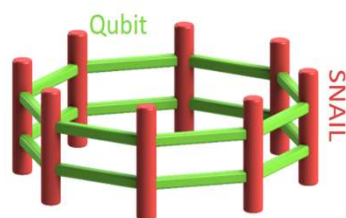
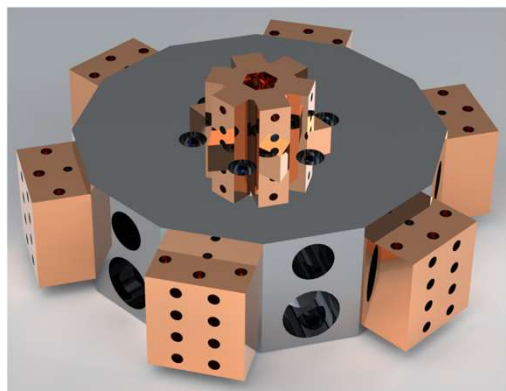
Next steps:

- Constraints for SNAIL-qubit conversion
- Multi-qubit gate + speed limits
- Scheduling pulses for double SNAILS

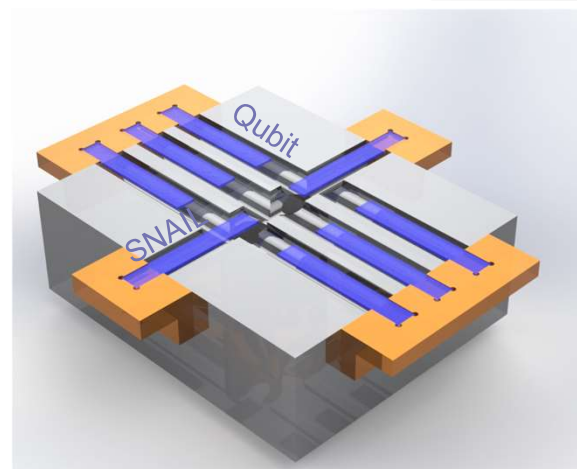
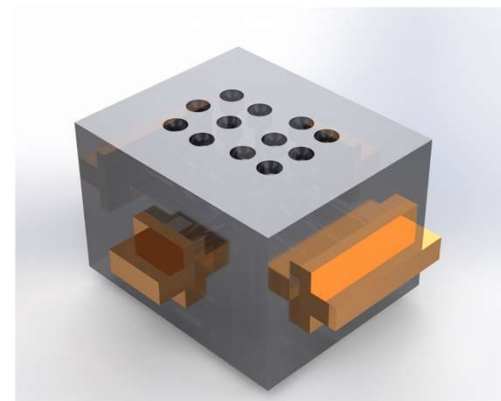
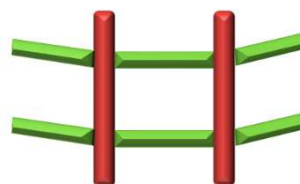
➤ Qubit bandwidth [4,6] GHz

Physical realization of the module (and potential problems?)

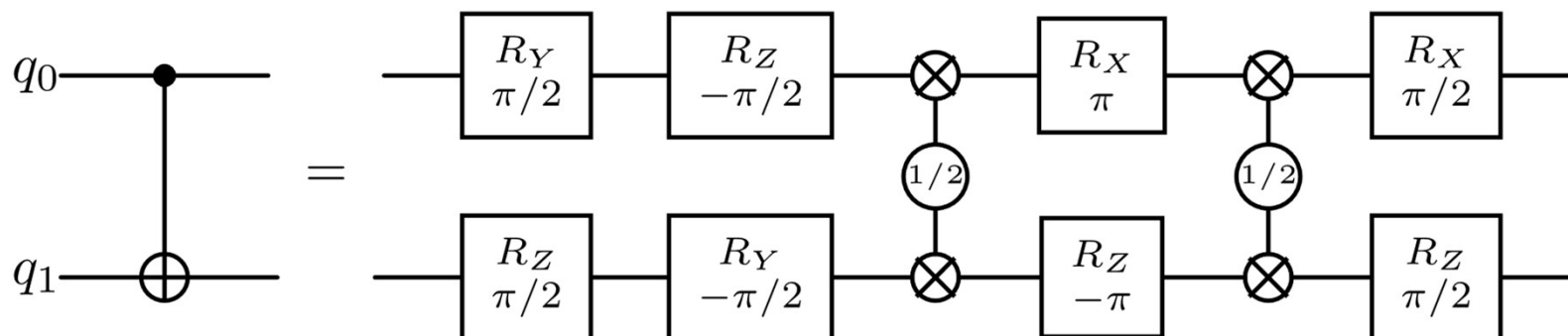
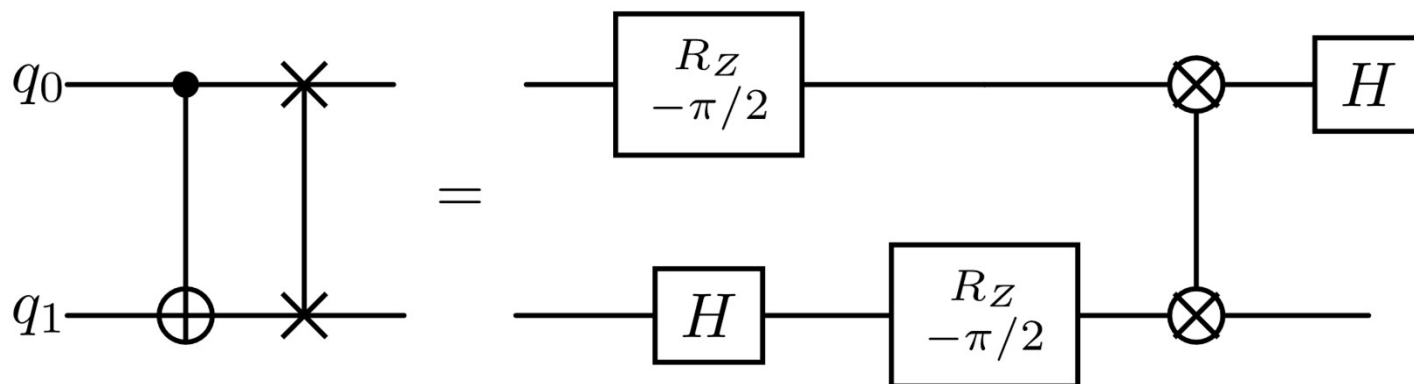
Corral



Fence-line



Decomposition identities



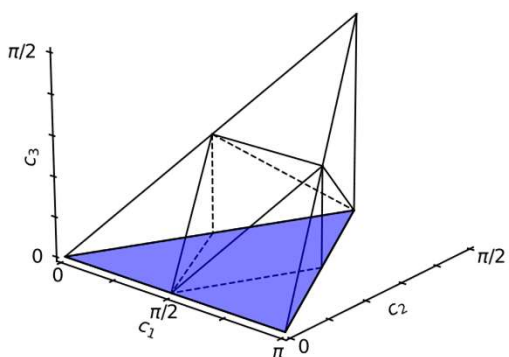
Schuch, et al. **Physical Review A** 67.3 (2003)
 Huang, et al. **Physical Review Letters** (2023)

McKinney, et al. **HPCA** (2024)

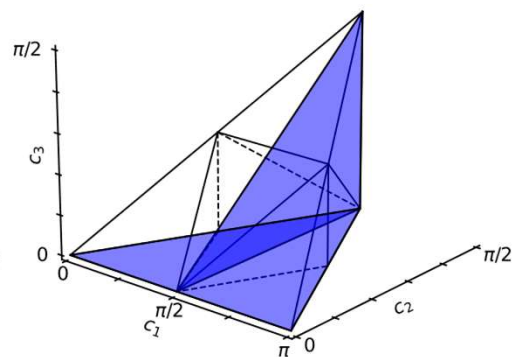
Mirror-inclusive coverage sets

- Compute effective coverage volumes using monodromy polytopes

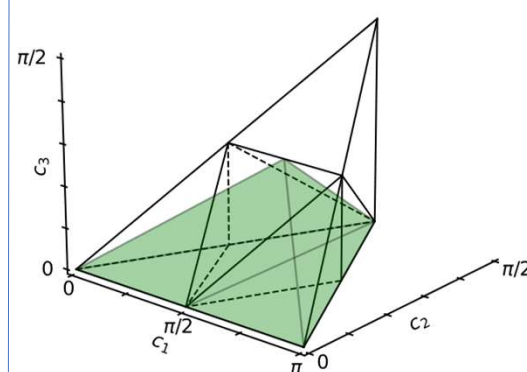
CNOT



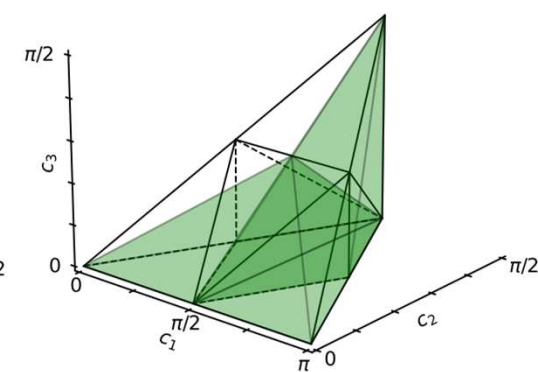
CNOT+Mirrors



\sqrt{i} SWAP



\sqrt{i} SWAP+Mirrors



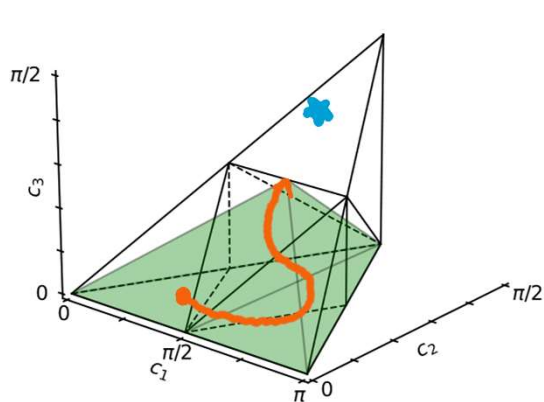
Peterson, et al. **Quantum 4** (2020)
 Peterson, et al. **Quantum 6** (2022)
 McKinney, et al. **HPCA** (2024)

$k = 2$

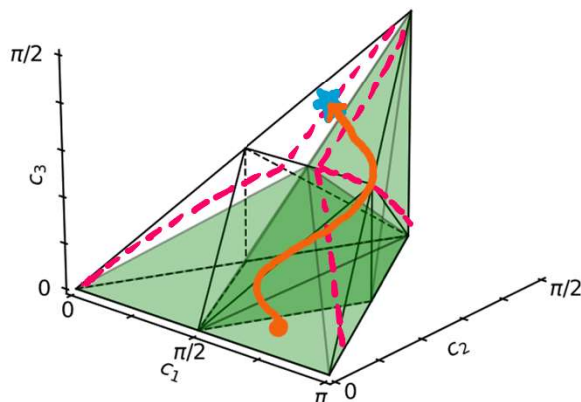
Monte Carlo Haar scores

➤ Intuition: Approximate decomp threshold defines an acceptable inflated polytope volume.

Javadi, Ali. **APS March Meeting** (2023)



Exact: Fail



Approx. + Mirrors: Success

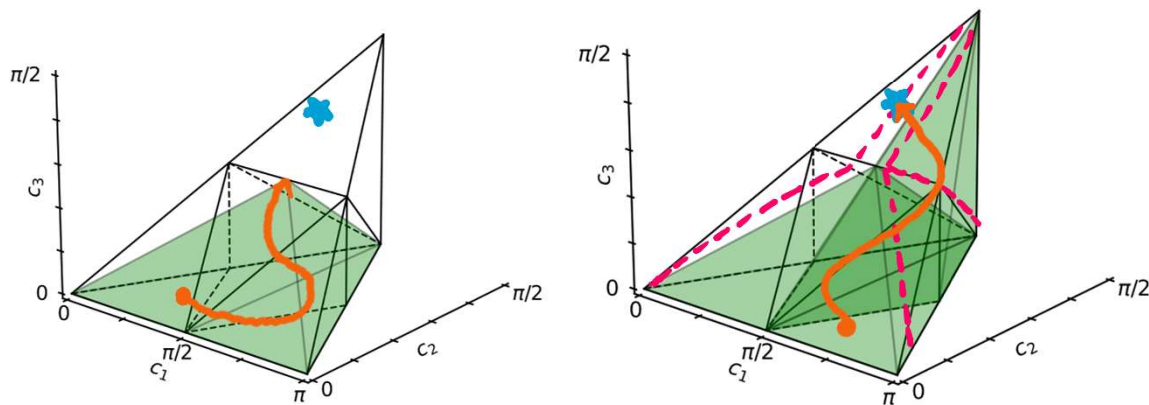
Lao, et al. **ISCA** (2021)

McKinney, et al. **HPCA** (2024)

Monte Carlo Haar scores

➤ Intuition: Approximate decomp threshold defines an acceptable inflated polytope volume.

Javadi, Ali. **APS March Meeting** (2023)



Exact: Fail

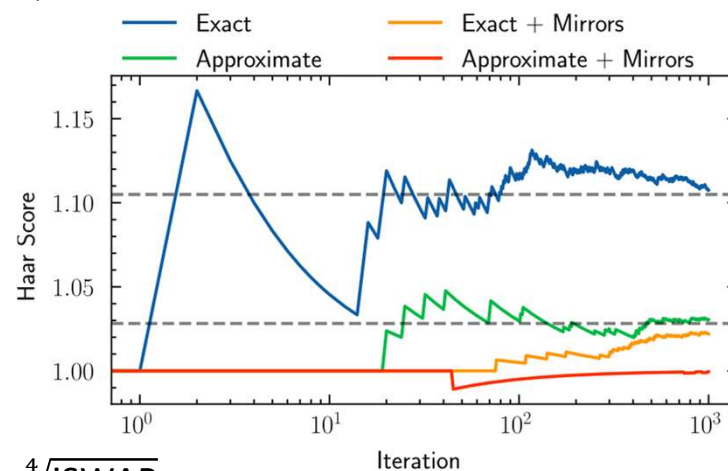
Approx. + Mirrors: Success

➤ \sqrt{i} SWAP with approximate decomp + mirrors has an 8.8% relative decrease in total infidelity

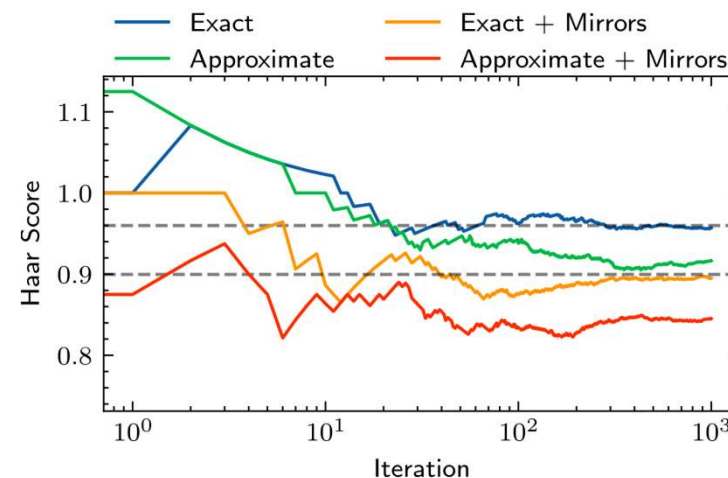
Lao, et al. **ISCA** (2021)

McKinney, et al. **HPCA** (2024)

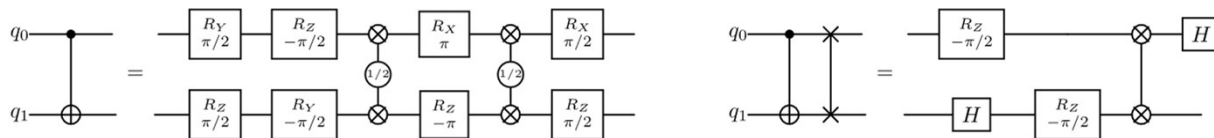
\sqrt{i} SWAP



$\sqrt[4]{i}$ SWAP

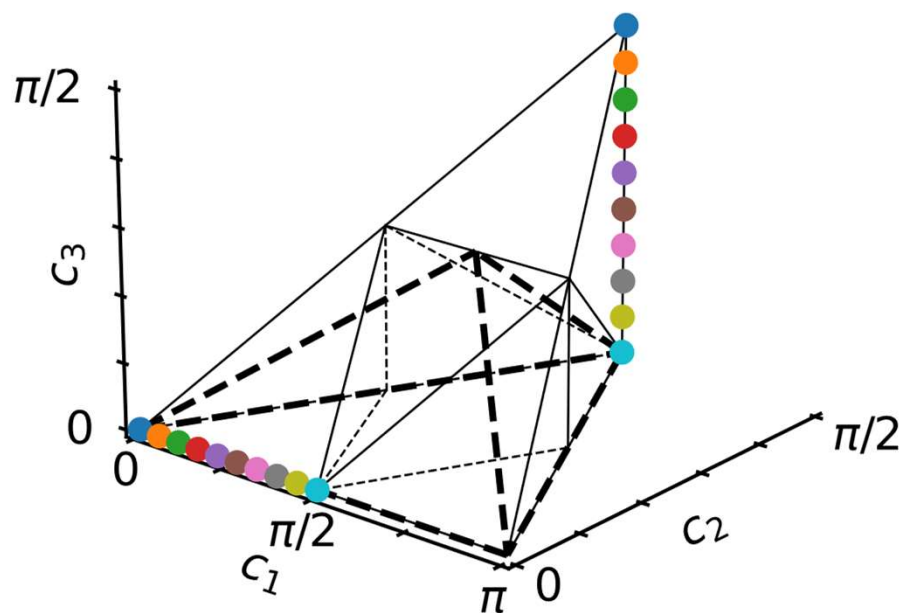


Why does this work?

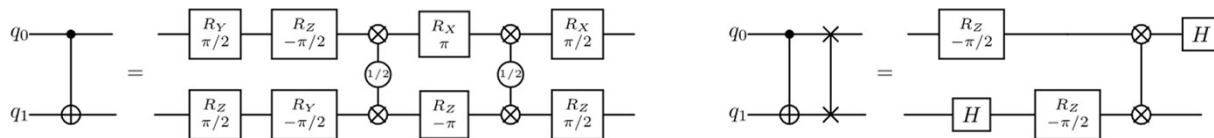


➤ CPHASE gates mirror to pSWAP gates

$$(a', b', c') = \begin{cases} (\frac{\pi}{4} + c, \frac{\pi}{4} - b, \frac{\pi}{4} - a) & \text{if } a \leq \frac{\pi}{4} \\ (\frac{\pi}{4} - c, \frac{\pi}{4} - b, a - \frac{\pi}{4}) & \text{else} \end{cases}$$

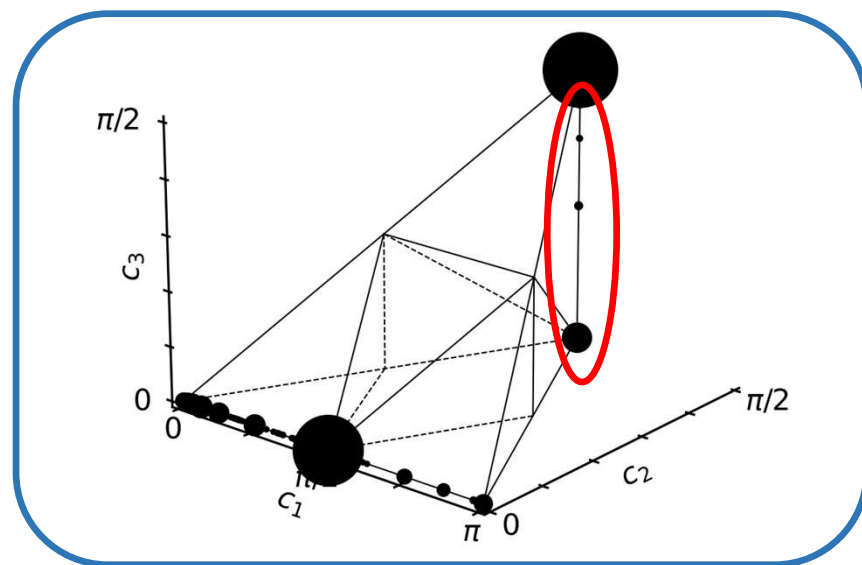
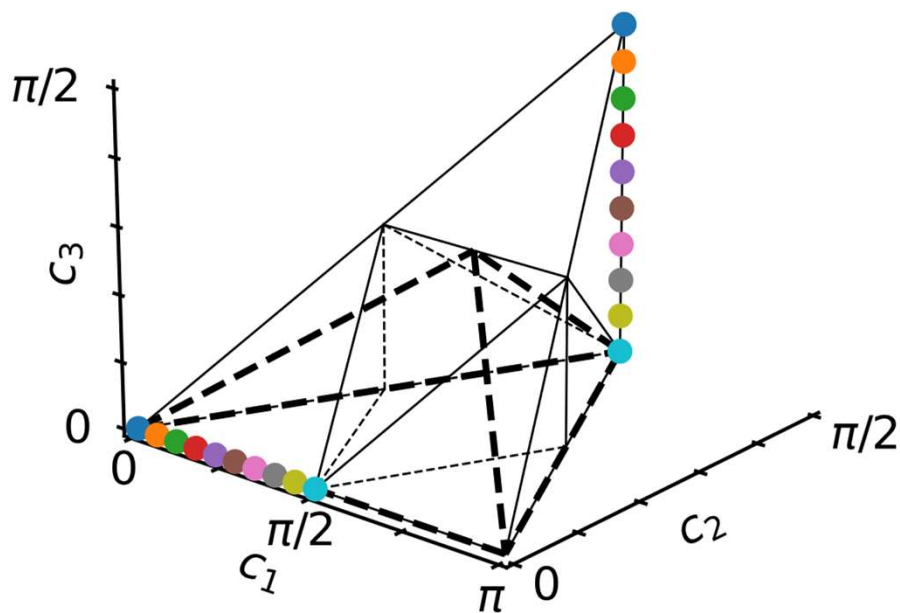


Why does this work?



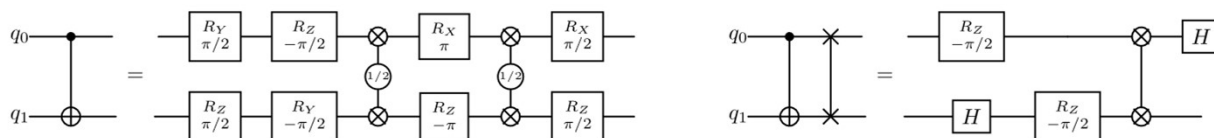
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$$(a', b', c') = \begin{cases} (\frac{\pi}{4} + c, \frac{\pi}{4} - b, \frac{\pi}{4} - a) & \text{if } a \leq \frac{\pi}{4} \\ (\frac{\pi}{4} - c, \frac{\pi}{4} - b, a - \frac{\pi}{4}) & \text{else} \end{cases}$$



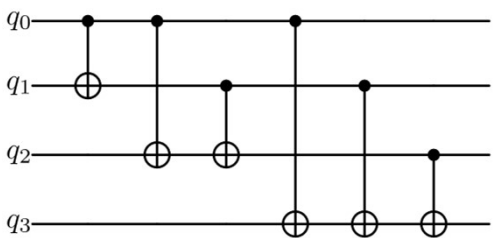


Using mirrors for data movement

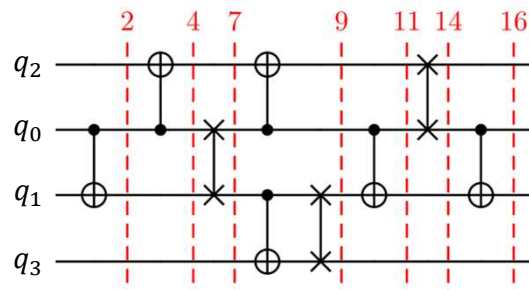


➤ Intuition: For every CX, decide whether output qubit ordering is (q_0, q_1) or (q_1, q_0) based on whether it makes the qubits closer to their next qubit pair

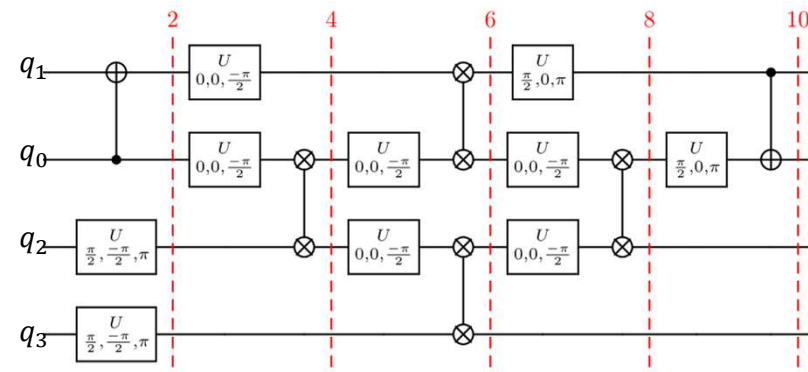
Goal: Full entanglement on a line topology



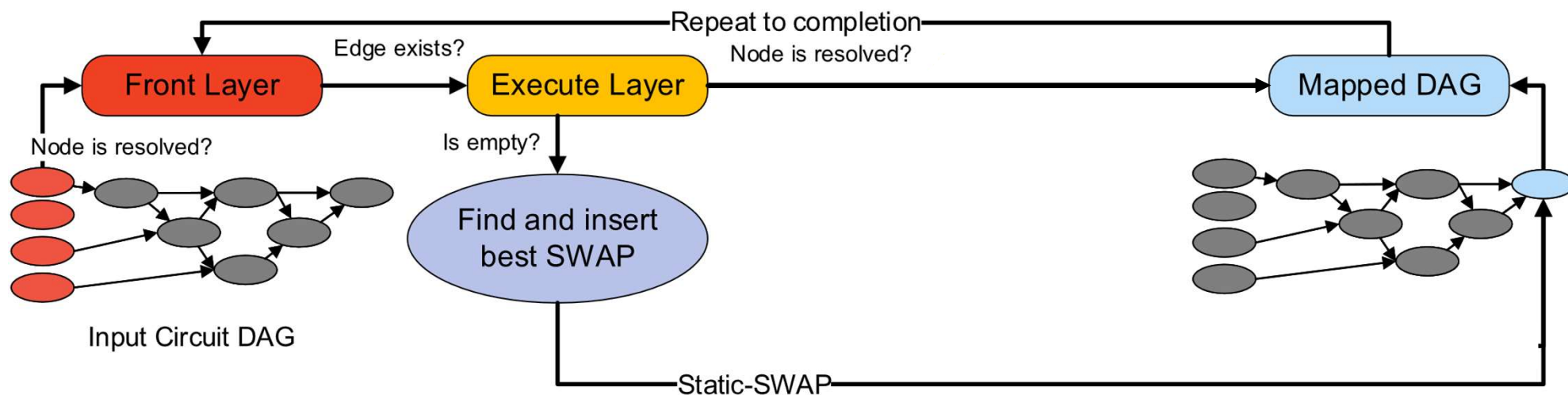
Qiskit



MIRAGE

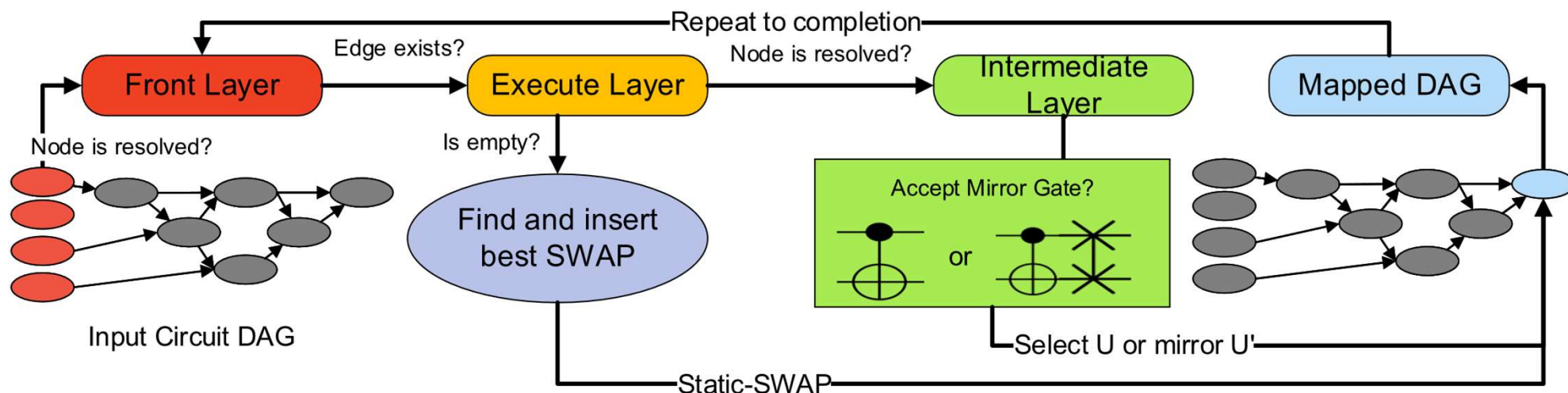


Mirage flow



- Simple yet powerful modification to SABRE:
 - Each gate must pass through an Intermediate Layer
 - Considers if substituting the *mirror* would reduce topological distance cost

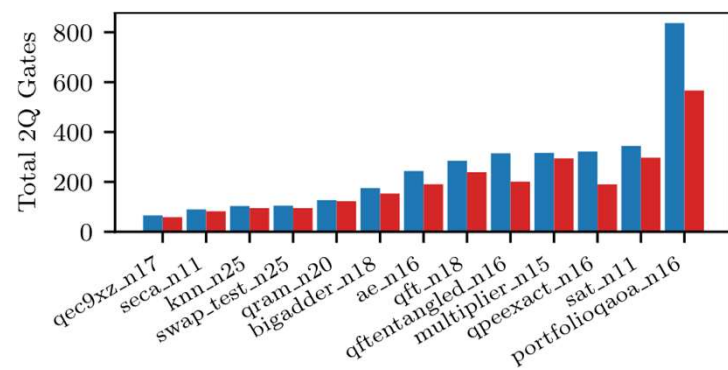
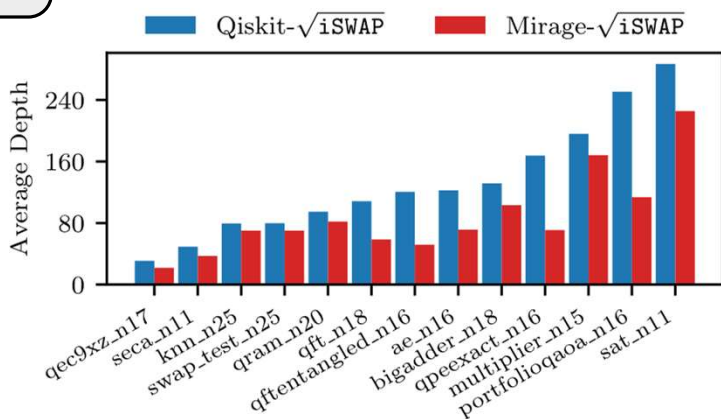
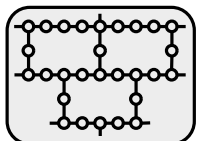
Mirage flow



- Simple yet powerful modification to SABRE:
 - Each gate must pass through an Intermediate Layer
 - Considers if substituting the *mirror* would reduce topological distance cost

Circuit depth reduction

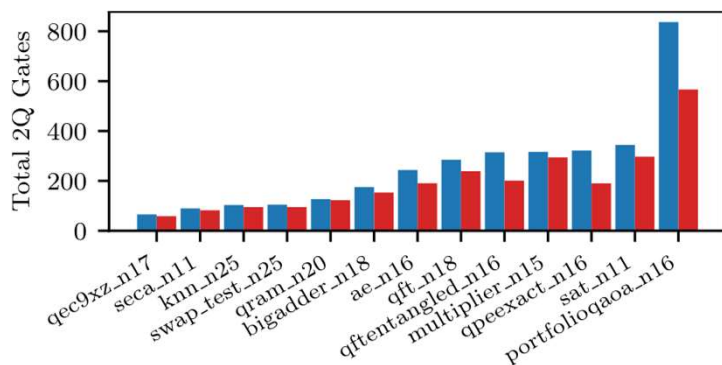
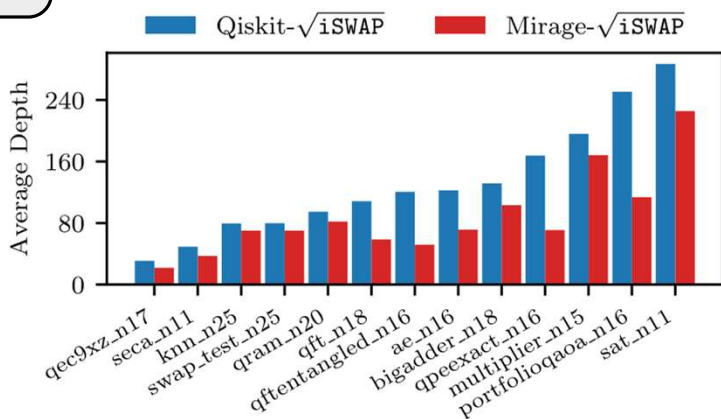
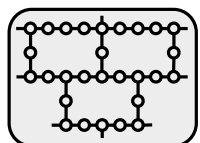
- For the Heavy-Hex topology
 - Average depth decrease of **31.19%**
 - Average total gate decrease of **16.97%**



Circuit depth reduction

➤ For the Heavy-Hex topology

- Average depth decrease of **31.19%**
- Average total gate decrease of **16.97%**



➤ Qiskit Transpiler Plugin

```

Usage

from qiskit.transpiler import CouplingMap
coupling_map = CouplingMap.from_grid(6, 6)

1. Use as a Qiskit-Plugin

Integrate MIRAGE into your existing transpilation pipeline:

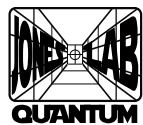
from qiskit import transpile
mirage_qc = transpile(
    qc, # input circuit
    optimization_level = 3, # default: Qiskit's highest level
    coupling_map=coupling_map,
    basis_gates= ["u", "xx_plus_yy", "id"],
    routing_method="mirage",
    layout_method="sabre_layout_v2",
)
    
```

➤ Software optimizations:

- Depth post-selection criteria
- Variable mirror acceptance thresholds
- Fast block consolidate w/ coord caching



<https://github.com/Pitt-JonesLab/mirror-gates>



Conclusions



- Evaluate $\sqrt{i\text{SWAP}}$ as a choice basis gate for optimized quantum ISAs
- Qubit frequency allocation over hardware-aware gate errors for SNAIL Corral design
- Significant circuit optimization with MIRAGE, **reducing depth by ~30%**



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